28F800BV/CV/CE
28F008BV/BE
SPECIFICATION UPDATE

Release Date: May 1997

Order Number 297688-006

The 28F800BV/CV/CE and 28F008BV/BE may contain design defects or errors known as errata. Characterized errata that may cause the 28F800BV/CV/CE and 28F008BV/BEs' behavior to deviate from published specifications are documented in this specification update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
01/16/96	-001	This document includes all items from the predecessor document *Errata/Addenda Information for 8-Mbit Boot Block SmartVoltage Flash Memories* (Order 297688-001): Errata: #9511001 5V Read Current Errata Documentation Change: Device Identifier
07/01/96	-002	This is the new format for the Specification Update document. It contains all identified errata published prior to this date.
05/15/96	-003	Spec Changes added: Reset Pulse Width, Reset to Data Float Time, t_{PHWL}/t_{PHEL} update, I_{OL}/I_{OH} spec change. Errata Revised: 5V Read Current increased from previous errata. New Errata: t_{WHWL2}/t_{EHEL2} Third Write Pulse, t_{AVWH} timing, t_{EHQZ}/t_{GHQZ} timing, Extended Temp Low-Voltage Programming
08/23/96	-004	New Errata: Boot block not locked on early 44-PSOP units
01/10/97	-005	C-step information added to: Errata - t_{PHWL}/t_{PHEL} Pushout Errata - Third-Write Pulse (affected prod) New Spec Changes: t_{PHQV}, t_{EHQZ} and t_{GHQZ} specifications changed
05/05/97	-006	Errata - t_{PHWL}/t_{PHEL} Pushout for A & B step @ 2.7V– 3.6V

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the sixth release of the 28F800BV/CV/CE and 28F008BV/BE Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *8-Mbit (512K x 16, 1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*.

Affected Documents/Related Documents

Title	Order
8-Mbit (512K x 16, 1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet	290539

Nomenclature

Errata are design defects or errors. These may cause the 28F800BV/CV/CE and 28F008BV/BEs' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the *8-Mbit (512K x 16, 1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet.* Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

Page:	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Item	Steppings			Page	Status	Errata
	A	B	C			
1	X			7	Eval	5V Read Current is higher than spec. Raised again in Revision 003.
2	X	X	X	8	NoFix	New t_{WHWL2}/t_{EHEL2} spec (Third Write-Pulse)
3	X			10	Fixed	t_{AVWH} timing issue in 2.7V and 3.3V ranges.
4	X			11	Fixed	t_{EHQZ}/t_{GHQZ} timing change in 5V V_{CC} range.
5	X			12	Eval	No program below 0°C at 3.3V V_{CC}, 44-PSOP.
6	X	X		13	Fixed	Boot Block not locked on early 44-PSOP units.
7	X	X	X	14	NoFix	t_{PHWL}/t_{PHEL} out of spec from 2.7V–3.6V V_{CC} operation on A, B & C-step material. 5V V_{CC} operation not affected.

Specification Changes

Item	Steppings	Page	Status	Specification Changes
	#			
1	All	15	Doc	t_{PLPH} specification definition and values
2	All	16	Doc	t_{PLQZ} specification definition and values
3	All	17	Doc	I_{OH}/I_{OL} spec change in 2.7V and 3.3V ranges
4	All	18	Doc	t_{EHQZ} and t_{GHQZ} specifications changed
5	All	18	Doc	t_{PHQV} changed in 2.7V and 3.3V ranges

Specification Clarifications

Item	Steppings	Page	Status	Specification Clarifications
	#			
		19		None in this Specification Update revision.

Documentation Changes

Item	Document Revision	Page	Status	Documentation Changes
1	290539-002	19	Doc	Device Identifier incorrect in -002 datasheet.

IDENTIFICATION INFORMATION

Markings

Stepping	Identifier
A-Step	1. Ninth digit of topside FPO mark (third line) = “A”
B-Step	1. Ninth digit of topside FPO mark (third line) = “B”
C-Step	1. Ninth digit of topside FPO mark (third line) = “C”

ERRATA

1. Read Current Increase in 5V Operation

PROBLEM: Affected material does not meet datasheet specifications for I_{CCR} when using V_{CC} in 5V range at either commercial or extended temperature. 2.7V or 3.3V operation is not affected. See the table below for the errata specs.

Parameter	Commercial				Extended				Unit
	CMOS		TTL		CMOS		TTL		
	Errata	Spec	Errata	Spec	Errata	Spec	Errata	Spec	
I_{CCR} (V_{CC} Read Current)	75	60	80	65	75	65	80	70	mA

IMPLICATION: The increased current requirements of affected devices may have an impact on power supply loading or battery life.

WORKAROUND: Ensure that system power supply and/or battery is sufficient to meet the increased current requirements.

STATUS: Plans to fix this erratum are under evaluation. For the steppings affected, see the Summary Table of Changes at the beginning of this section.

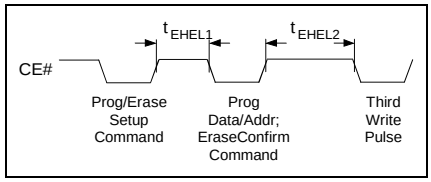
Update: Revision -003 increases errata currents by 5 mA each (already reflected in the table).

AFFECTED PRODUCTS: All A-step material operating V_{CC} at 5V is affected. V_{CC} at 2.7V or 3.3V is not affected.

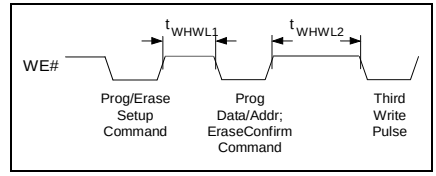
These products are affected. . .				. . .under these operating conditions		
Name	Package	Step	Marking	V_{CC}	V_{PP}	Temp
E28F008BV-T/B, PA28F800BV-T/B, E28F800CV-T/B, TE28F008BV-T/B, TB28F800BV-T/B, TE28F800CV-T/B, TE28F008BE-T/B, TE28F800CE-T/B, AB28F800BR-T/B	All	A	Ninth digit of topside FPO mark (third line) equals “A”	5V ± 5% 5V ± 10%	All	All

2. Third Write-Pulse t_{WHWL2}/t_{EHEL2} New Specification

PROBLEM: This specification affects designs issuing program or erase commands to the flash device with V_{CC} = 3.3 ± 0.3V or 2.7V–3.6V. Operation with V_{CC} = 5V ± 10% is not affected. Program and erase functions are initiated using a two-write sequence, with the program or erase setup command being written to the part, then the data program or erase confirm being written on the next cycle after a time t_{WHWL1} (t_{EHEL1} for CE#-controlled writes) between the write low pulses. Following the second write in a two-write sequence; the WE# (CE#) signal must stay high for a time t_{WHWL2} (t_{EHEL2}) before going low again for a third write pulse. This is shown as the t_{WHWL2} (t_{EHEL2}) on the right in the timing diagram below. The value of t_{WHWL1} (t_{EHEL1}) between the first and second write in the sequence remains at its current specification. The specified and erratum values are shown in the table which follows.



Timing Waveform
Showing Two t_{WHWL} Specifications



Timing Waveform
Showing Two t_{EHEL} Specifications

New Write Specifications: Commercial Temperature

Write Control	Parameter	Product	BV–70	BV–120	Unit
		V_{CC}	3.3 ± 0.3V		
		Load	50 pF		
			Min	Min	
WE#-Controlled Writes	t_{WHWL1} (Second write)		20	30	ns
	t_{WHWL2} (Third write)		40	40	ns
CE#-Controlled Writes	t_{EHEL1} (Second write)		20	30	ns
	t_{EHEL2} (Third write)		40	40	ns

New Write Specifications: Extended Temperature

Write Control	Parameter	Product	TBE–120	TBV–90	Unit
		V_{CC}	2.7V–3.6V	3.3V ± 0.3V	
		Load	50 pF		
			Min	Min	
WE#-Controlled Writes	t_{WHWL1} (Second write)		30	20	ns
	t_{WHWL2} (Third write)		40	40	ns
CE#-Controlled Writes	t_{EHEL1} (Second write)		30	20	ns
	t_{EHEL2} (Third write)		40	40	ns

IMPLICATION: Violating the specified conditions described can cause the Write State Machine to abort the program or erase operation in progress and report a successfully completed operation in the Status Register, although in reality, the operation has not completed successfully.

WORKAROUND: Note, however, that it is not useful for the system to write to the flash device after a program sequence until the Status Register reports that the program operation has completed, since the State Machine is designed to ignore all instructions while a program operation is in progress. Writing the Status Register read command to the device is not necessary since the device defaults to outputting Status Register data while the program operation is in progress. In the case of an erase operation, the only valid command that should be written to the device while an erase operation is in progress is the erase suspend command. In this situation, the system must wait for the specified value of t_{WHWL2} (t_{EHEL2}) before requesting an erase suspend.

STATUS: No fix is planned for this erratum. For the steppings affected, see the Summary Table of Changes at the beginning of this section.

AFFECTED PRODUCTS: All A-step, B-Step, and C-step material operating V_{CC} at 2.7V–3.6V or 3.3V ± 0.3V is affected. V_{CC} at 5V is not affected.

These products are affected. . .				. . .under these operating conditions		
Name	Package	Step	Marking	V_{CC}	V_{PP}	Temp
E28F008BV-T/B, PA28F800BV-T/B, E28F800CV-T/B, TE28F008BV-T/B, TB28F800BV-T/B, TE28F800CV-T/B, TE28F008BE-T/B, TE28F800CE-T/B,	All	A B C	Ninth digit of topside FPO mark (third line) equals “A” , “B” or “C”	2.7V–3.6V 3.3 ± 0.3V	All	All

3. t_{AVWH} Timing in 2.7V and 3.3V Ranges

PROBLEM: Affected material does not meet datasheet specifications for t_{AVWH} when operating with V_{CC} = 2.7V–3.6V or V_{CC} = 3.3V ± 0.3V in either the commercial or extended temperature range. t_{AVWH} specifies the time that the address lines must be stable before the WE# signal goes high. See the table below for the errata specs.

Write Specification Erratum: Commercial Temperature

Write Control	Parameter	Product	BV–70		Unit
		V_{CC}	3.3V ± 0.3V		
		Load	50 pF		
			Errata	Spec	
WE#-Controlled Writes	t_{AVWH} (Addr Setup to WE# Going High)		130	90	ns

Write Specification Erratum: Extended Temperature

Write Control	Parameter	Product	TBE–120/TBV–90		Unit
		V_{CC}	2.7V–3.6V or 3.3V ± 0.3V		
		Load	50 pF		
			Errata	Spec	
WE#-Controlled Writes	t_{AVWH} (Addr Setup to WE# Going High)		130	90	ns

IMPLICATION: The timing between the address lines and WE# may need to be re-evaluated to see if the errata spec causes any timing issues.

WORKAROUND: Ensure that the memory interface timing meets these requirements.

STATUS: This errata has been fixed in the B-stepping of this product. For the steppings affected, see the Summary Table of Changes at the beginning of this section.

AFFECTED PRODUCTS: All A-step material operating V_{CC} at 2.7V–3.6V or 3.3V ± 0.3V is affected. V_{CC} at 5V is not affected.

These products are affected. . .				. . .under these operating conditions		
Name	Package	Step	Marking	V_{CC}	V_{PP}	Temp
E28F008BV-T/B, PA28F800BV-T/B, E28F800CV-T/B, TE28F008BV-T/B, TB28F800BV-T/B, TE28F800CV-T/B, TE28F008BE-T/B, TE28F800CE-T/B, AB28F800BR-T/B	All	A	Ninth digit of topside FPO mark (third line) equals “A”	2.7V–3.6V 3.3 ± 0.3V	All	All

4. t_{EHQZ}/t_{GHQZ} Timing in 5V Range

PROBLEM: Affected material does not meet datasheet specifications for t_{EHQZ} and t_{GHQZ} when operating with V_{CC} = 5V ± 5% or 5V ± 10% in the commercial temperature range. t_{EHQZ} specifies the latency between when CE# goes high to when the flash output drivers go to high-impedance. t_{GHQZ} specifies the latency between when OE# goes high to when the flash output drivers go to High-Z. See the table below for the errata specs.

Read Specification Erratum: Commercial Temperature

Parameter	Product	BV–70				Unit
	V_{CC}	5V ± 5%		5V ± 10%		
	Load	30 pF		100 pF		
		Errata	Spec	Errata	Spec	
t_{EHQZ} (CE# High to Output High-Z)		30	20	30	25	ns
t_{GHQZ} (OE# High to Output High-Z)		25	20	25	25	ns

IMPLICATION: The errata specs indicate that the flash device is taking longer to get off the data bus than originally specified. This can cause bus conflict between the flash memory and the microprocessor if the processor begins driving the bus before the flash is off.

WORKAROUND: Ensure that the memory interface timing meets these requirements. Adjustments to the processor timing may be necessary.

STATUS: This errata is under evaluation. For the steppings affected, see the Summary Table of Changes at the beginning of this section.

AFFECTED PRODUCTS: All –70 ns A-step material operating V_{CC} at 5V is affected. Extended temperature products and V_{CC} operation at 3.3V is not affected.

These products are affected. . .				. . .under these operating conditions		
Name	Package	Step	Marking	V_{CC}	V_{PP}	Temp
E28F008BV-T/B, PA28F800BV-T/B, E28F800CV-T/B	All	A	Ninth digit of topside FPO mark (third line) equals “A”	5V ± 5% 5V ± 10%	All	Commercial

5. Extended Temperature Programming Limitations

PROBLEM: Affected material has the following limitations on operating parameters:

Parameter	Min	Max	Unit
Extended Temperature Range (Program only)	0	+85	°C

Because on-chip program circuitry is sensitive to very low temp operation, this material must be programmed within the temperature range of 0°C to +85°C. Read and erase operation is unaffected over the full extended temperature operating range (–40°C to +85°C).

IMPLICATION: This erratum limits the temperature range over which affected material can be programmed.

WORKAROUND: Contact your Intel representative for workaround information.

STATUS: This errata has been fixed on the B-stepping of the device. For the steppings affected, see the Summary Table of Changes at the beginning of this section.

AFFECTED PRODUCTS: All A-step material operating V_{CC} at 2.7V–3.6V or 3.3V ± 0.3V is affected. Operation at 5V is not affected.

These products are affected. . .				. . .under these operating conditions		
Name	Package	Step	Marking	V_{CC}	V_{PP}	Temp
TB28F800BV-T/B	44-PSOP	A	Ninth digit of topside FPO mark (third line) equals “A”	3.3 ± 0.3V	All	Extended

6. Boot Block Not Locked on Initial 44-PSOP Units

PROBLEM: Affected material does not lock the 16-Kbyte boot block when RP# = V_{IL} or V_{IH} to protect it from write or erase operations. The 16-Kbyte boot block should be locked under these RP# conditions. Consequently, the boot block is not lockable using any control signals and is permanently unlocked.

For further details on the boot block locking function, please refer to Section 3.4 and Table 9 in the *8-Mbit (512K x 16, 1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*.

IMPLICATION: Because the boot block is unlocked, any write or erase command into the boot block will be successfully carried out regardless of the RP# input.

WORKAROUND: Please work with your Intel sales representative to facilitate return and replacement of the affected material, if you so desire.

STATUS: Intel has fixed the issue in manufacturing and began shipping fixed material during the week of June 24, 1996. For the steppings affected, see the Summary Table of Changes at the beginning of this section.

AFFECTED PRODUCTS: All 44-PSOP package material with third and fourth digit of topside FPO mark (third line) less than or equal to 24 are affected.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
PA28F800BVT70 PA28F800BVB70 PA28F800BVT120 PA28F800BVB120 TB28F800BVT90 TB28F800BVB90	44-PSOP	A B	Third and fourth digit of topside FPO mark (third line) ≤ 24	All	All	All

Any 44-PSOP package material with third and fourth digit of topside FPO mark (third line) greater than 24 is not affected.

7. t_{PHWL}/t_{PHEL} Pushout

PROBLEM: Affected material does not meet its t_{PHWL}/t_{PHEL} specification for write operations in 2.7V and 3.3V V_{CC} operations. A, B, and C-step material is not affected at 5V V_{CC} operations.

Specification	V_{CC} = 3.3 ± 0.3V V_{CC} = 2.7V–3.6V	V_{CC} = 5V ± 10%	Units
t_{PHWL} /t_{PHEL}(Datasheet)	1.5	0.45	µs
t_{PHWL} /t_{PHEL}(C-step Erratum)	25	meets spec	µs

The specification t_{PHWL} (RP# High Recovery to WE# Going Low) is the minimum time between the RP# signal going high to WE# going low. The specification t_{PHEL} (RP# High Recovery to CE# Going Low) is the minimum time between the RP# signal going high to CE# going low.

IMPLICATION: The erratum affects the delay from coming out of a reset until a command write can be executed on the part (affects both WE#-controlled and CE#-controlled command sequences). Although the read specification t_{PHQV} (RP# going high to data valid) Is less than the t_{PHWL}/t_{PHEL} errata, the full time for t_{PHWL}/t_{PHEL} must be completed prior to WE# going low.

WORKAROUND: Verify system timings to ensure this does not impact your design.

STATUS: This erratum pushes-out A, B, and C-step material. It meets specification when operating at 5V, but does not meet specification for 2.7V and 3V operations. No fix or further improvement is planned.

AFFECTED PRODUCTS: This erratum applies to A, B, and C-step material.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F008BV-T/B, PA28F800BV-T/B, E28F800CV-T/B, TE28F008BV-T/B, TB28F800BV-T/B, TE28F800CV-T/B, TE28F008BE-T/B, TE28F800CE-T/B, AB28F800BR-T/B	All	A B C	Ninth digit of topside FPO mark (third line) equals “A” , “B” or “C”	2.7-3.6	All	All

SPECIFICATION CHANGES

1. New t_{PLPH} Specification Definition and Values

PROBLEM: This item defines a new specification that will be added to the datasheet. This specification is t_{PLPH} and is defined as the minimum time that RP# must be held low in order to produce a valid reset of the device.

The table below lists t_{PLPH} specification values.

Specification	Vcc		Units
	3.3V ± 0.3V 2.7V-3.6V	5V ± 10%	
t_{PLPH} - Reset Pulse Width (Minimum)	150	60	ns

Timing Diagram for t_{PLPH} Specification

IMPLICATION: Systems that are not asserting the reset signal low longer than t_{PLPH} may not be properly resetting the flash component.

AFFECTED PRODUCTS: This specification is applicable to all products covered by this document.

2. New t_{PLQZ} Specification Definition and Values

PROBLEM: This item defines a new specification that will be added to the datasheet. This specification is t_{PLQZ} and is defined as the maximum time after RP# goes to logic low until the flash data pins go to high-impedance state. The table below lists t_{PLQZ} specification values (typical output loads).

AC Characteristics: Read Only Operations

Specification	V_{CC}		Units
	3.3V ± 0.3V 2.7V–3.6V	5V ± 10%	
t_{PLQZ} - RP# Low to Output High Z (Maximum)	150	60	ns

Timing Diagram for t_{PLQZ} Specification

IMPLICATION: Because the flash requires a time t_{PLQZ} after reset goes low until the data pins go to high-impedance, systems that do not meet this specification may have problems with bus contention.

AFFECTED PRODUCTS: This specification is applicable to all products covered by this document.

3. I_{OH}/I_{OL} Specification Change in 2.7V and 3.3V Ranges

PROBLEM: The output current specs I_{OH}/I_{OL} are being changed from their datasheet specifications. I_{OH}/I_{OL} are specified in the test conditions column of the V_{OL}, V_{OH1}, and V_{OH2} rows of the DC Characteristics table. The table below details the changes made to the DC Characteristics table of the datasheet.

	Sym	Parameter	V_{CC} 3.3 ± 0.3V 2.7-3.6V		Unit	Test Conditions
			Min	Max		
Before	V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = V_{CC}$ MIN, I_{OL} = 5.8 mA
After	V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = V_{CC}$ MIN, **I_{OL} = 2.0 mA**
Before	V_{OH1}	Output High Voltage (TTL)	2.4		V	$V_{CC} = V_{CC}$ MIN, I_{OH} = –2.5 mA
After	V_{OH1}	Output High Voltage (TTL)	2.4		V	$V_{CC} = V_{CC}$ MIN, **I_{OH} = –2.0 mA**
Before	V_{OH2}	Output High Voltage (CMOS)	0.85 x V_{CC}		V	$V_{CC} = V_{CC}$ MIN, I_{OH} = –2.5 mA
After	V_{OH2}	Output High Voltage (CMOS)	0.85 x V_{CC}		V	$V_{CC} = V_{CC}$ MIN, **I_{OH} = –2.0 mA**

IMPLICATION: This change can impact the number of devices that can be driven from the outputs of the flash memory (reduced fan out) due the reduced output current specs.

AFFECTED PRODUCTS: This specification is applicable to all products covered by this document.

4. t_{EHQZ} and t_{GHQZ} Specification Change

PROBLEM: This item changes the specifications t_{EHQZ} and t_{GHQZ}, which define how long the flash takes to get off the bus after the outputs are disabled. t_{EHQZ} specifies the latency between when CE# goes high to when the flash output drivers go to high-impedance. t_{GHQZ} specifies the latency between when OE# goes high to when the flash output drivers go to High-Z. The following table defines the new spec values, which will be included in the *1997 Flash Memory Databook*.

Read Specification Update: Commercial and Extended Temperature

	V_{CC}	2.7V-3.6V or 3.3 ± 0.3V	5V ± 5%	5V ± 10%	
Parameter		**New Spec**	**New Spec**	**New Spec**	**Unit**
t_{EHQZ} (CE# High to Output High-Z)		45	20	25	ns
t_{GHQZ} (OE# High to Output High-Z)		55	20	25	ns

IMPLICATION: This spec change can eliminate the need for a bus transceiver in higher frequency designs, depending on the specific processor-memory interface.

AFFECTED PRODUCTS: This change applies to all speeds of the 28F008/800BV/CV/BE/CE products at both commercial and extended temperature.

5. t_{PHQV} Specification Change

PROBLEM: This item changes the specifications t_{PHQV}, has been changed to 0.8 µs from their datasheet value of 1.5 µs, when operating with V_{CC} in the 2.7V–3.6V or 3.3V ± 0.3V ranges. The new values are shown in the table below.

Specification	**V_{CC}**		**Units**
	3.3V ± 0.3V 2.7V–3.6V	**5V ± 10% 5V ± 5%**	
t_{PHQV} (Datasheet)	1.5	0.45	µs
t_{PHQV} (Changed)	0.8	0.45	µs

The specification t_{PHQV} (RP# High Recovery to Output Delay) is the minimum time between the RP# signal going high to when data is valid on the outputs.

IMPLICATION: The specification affects the delay from coming out of a reset until valid data can be read on the outputs.

AFFECTED PRODUCTS: This change applies to all speeds of the 28F008/800BV/CV/BE/CE products at both commercial and extended temperature.

SPECIFICATION CLARIFICATIONS

There are no specification clarifications in this Specification Update revision.

DOCUMENTATION CHANGES

1. Device Identifier Incorrect in Revision -002, 8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet

PROBLEM: An error was made in the listing for the Intelligent Identifier device codes for the 28F008BV and 28F008BE products in Revision 002 of the *8-Mbit (512K x 16, 1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*. In Section 3.2.2, Table 5, the device IDs are listed incorrectly. The device IDs for the 28F800 products are correct. The correct device IDs for 28F008B products are 98H and 99H, for top and bottom boot, respectively. The correct device ID table is shown below:

Corrected Intelligent Identifier Table

Product	Manufacturer ID	Device ID	
		Top Boot (-T)	Bottom Boot (-B)
28F800BV/CV/CE	0089 H	889C H	889D H
28F008BV/BE	89 H	98 H	99 H

Revision -003 of the *8-Mbit (512K x 16, 1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* has been corrected.