AP-640

APPLICATION NOTE

Interfacing the 80186EB/EC Embedded Processor to Intel Boot Block Flash

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CONTENTS

REVISION HISTORY

Number	Description
-001	Original Version

1.0 INTRODUCTION

The 80C186EB and 80C186EC are the highest integration members of the 186 Integrated Processor Family. They represent a new generation of low-power, high-integration embedded microprocessors. These processors enhance the existing 186 family by offering new features and new operating modes. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface, and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The three general purpose timer/counters can be used for a variety of time measurement and waveform generation tasks. The 80C186EC provides additional features including four independent DMA channels and two 8259A compatible interrupt controllers.

The 80L186EB/EC is the 3V version of the 80C186EB/EC. The 80L186EB/EC is functionally identical to the 80C186EB/EC embedded processor. Current 80C186EB/EC users can easily upgrade their designs to use the 80L186EB/EC and benefit from the reduced power consumption inherent in 3V operation.

The feature set of the 80186EB/EC meets the needs of low-power, space-critical applications. Low-power applications benefit from the static design of the CPU and the integrated peripherals as well as low voltage operation. Minimum current consumption is achieved by providing a power-down mode that halts operation of the device and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

As embedded system designers take advantage of DOS capability in the PC platform, a revolutionary system architecture is required to meet space and power requirements.

- An architecture that is not bound by what has been done before with existing memory architecture, but free to meet the demanding requirements of embedded end-users.
- An architecture free to adopt and accommodate new technological advances in software and hardware, while protecting end-users initial base hardware investment.

Implementing this new system architecture requires an alternative to the traditional PC storage media such as ROM, DRAM, floppy disk, and hard disk. The solution is Intel's Boot Block Flash memory.

Intel Flash memory provides in-system program capabilities, along with selective block erase and program/erase automation which have gained wide acceptance in the embedded market. These features help with cost-effective field updates and provide quick time-to-market solutions in most applications.

By combining flash memory with this new system architecture, completely new types of designs are now possible that replace or integrate many of the code or storage functions of other memory types. Flash memory can be used for storing eXecute-In-Place (XIP) code in the system's memory map while additionally functioning like a disk for file and program storage. Since this type of design features flash memory resident on the embedded system's motherboard which is typically arranged in an array, it is described as a Resident Flash Array (RFA).

1.1 Embedded Memory Systems

The ideal embedded memory system is:

- Power Conscious (prolongs battery life and reduces heat)
- Dense (stores a large amount of code and data in a small amount of space but weighs very little)
- Updateable (allows in-system code enhancements)
- Fast (data is read and written quickly)
- Inexpensive (low cost-per-megabyte)
- Reliable (retains data when exposed to extreme temperature and mechanical shock)

Designers have grappled with how to construct memory systems that meet the above criteria. Embedded computing makes the system design even tougher with more stringent requirements for low power, low volume, less weight, and harsh environments. The best combination available for embedded designs in their infancy was the same as used for the desktop PC: solid-state memory and magnetic storage, e.g., SRAMs, DRAMs plus magnetic hard disks. DRAMs are dense and inexpensive, yet slower than the processors they serve, and they are volatile. SRAMs, although fast enough to keep pace with processors, are relegated to caching schemes (compensating for DRAM's slowness) due to low density and high cost while also being volatile. Magnetic hard disks are dense, inexpensive on a cost-per-megabyte basis, and nonvolatile. However, they are also slow, power-hungry, susceptible to damage from physical shock, and take up a sizable amount of volume.

Embedded computing designs cannot depend on hard drives as do desktop or portable PCs, due to size limitations. Furthermore, vitally important data such as credit card numbers or transactions, signatures, or patient monitoring information demands reliability of the highest order. The solution is Intel Flash memory.

1.2 The Flash Memory Alternative

High Density

Intel's ETOX™ IV flash memory cell is 30% smaller than equivalent DRAM cells; therefore, it will closely track DRAM density. Flash memory is more scaleable than DRAM because the flash storage cell is not sensitive to soft error failure; therefore, it can have a simpler cell structure. As density increases and process lithography continues to shrink, flash memory will pace, and ultimately overtake, the DRAM technology treadmill.

Updateable

ROMs and EPROMs may offer lower device costs, but overall system cost must be factored in if servicing the customer or end-user is important to an OEM. Although ROMs and EPROMs are nonvolatile, changing the code within them is either very difficult (in the case of EPROMs), or entirely impossible (in the case of ROMs). Whole inventories of ROMs could be made obsolete in the event of a catastrophic bug, while an innovative design with flash memory could be updated in the factory or by end-users via networks, OEM Bulletin Board Systems, web sites or other memory cards. Updating systems could actually become a second source of income for OEMs and Independent Software Vendors (ISVs), enhancing the quality of the product while increasing end-user satisfaction.

Power Conscious

Intel's flash memory provides a deep power-down mode, reducing power consumption to typically less than 0.2 µA. Typical read current is only 20 mA, while typical standby current (flash memory not being accessed with CE# high) is only 30 µA. Additionally, flash devices operating as low as 2.7V are available for state-of-the art low-power consumption designs.

Fast

Do not be misled by technology-to-technology speed comparisons. Architecting a system around flash memory bypasses the code/data bottleneck created by connecting slow mechanical serial memory (such as disks) to a high-performance, parallel bus system. For example, data seek time for a 1.8" magnetic hard disk is 20 ms, plus an 8 ms average rotational delay, while flash memory write time is less than 0.1 ms. At the chip level, read speeds for some flash memory products are about 70 ns. Therefore, either direct execution of code from flash memory or downloading to system RAM will dramatically enhance overall system performance.

Nonvolatile

Unlike DRAM or SRAM, flash memory requires no battery back-up. Furthermore, Intel's flash devices retain data well beyond the useful lifetime of most applications.

Rugged and Reliable

On average, today's hard-disk drives can withstand up to 10 Gs of operating shock. Intel's flash memory can withstand as much as 1000 Gs. Flash components can operate beyond +70°C while magnetic drives are limited to +55°C. Intel's flash memory can be cycled 100,000 times per block or segment. By employing wear-leveling techniques, the cycling of a device can be minimized. For example, a 10-KB file written every 5 minutes, 24-hours a day to a 20-MB flash array takes 16 million hours, or 1826 years, before reaching the 100,000 cycle level.

1.3 Summary

Many embedded applications benefit from ROMed or XIP versions of code, particularly hand-held personal computers, vertical application pen-based clipboards, cellular phones, and industrial control and data accumulation equipment. These applications pose system design constraints requiring small form factor, low-power consumption, and rugged construction due to active mobile users or harsh environments. Exposure to shock, vibration, or temperature extremes is common, precluding the use of rotating media. Flash memory provides an excellent code storage choice for such system designs featuring thin TSOP packaging, low (deep power-down mode) or zero (capability to shut off power without losing data) power

consumption, 1000 G shock resistance, and extended temperature products. Additionally, flash memory provides remote or end-user update capability allowing OEMs to service their products more efficiently and add new software features and applications after the sale.

Compared to RAMs and ROMs, the timing requirements for flash are slightly different. This application note explores those differences and provides a detailed analysis of the interface between the 28Fx00B5/BV Boot Block flash memory family and the 80186EB/EC embedded microprocessor. Also discussed are the issues involved with designing the required interface.

2.0 FLASH TIMING PARAMETERS

The read and write timing parameters provided in Tables 1 through 5 are the most significant parameters involved with interfacing to Intel's Boot Block flash memory components.

Table 1. Read Timing Parameters (V_{CC} = 5V ± 10%)(1)

Timing Description	28F800BV-120	28F800BV-70 28F800B5-70	28F400BV-120	28F400BV-80 28F400B5-80	28F400BV-60 28F400B5-60
Address Valid to Data Valid, t_{AVQV} (max)	120 ns	80 ns	120 ns	80 ns	70 ns
CE# Valid to Data Valid, t_{ELQV} (max)	120 ns	80 ns	120 ns	80 ns	70 ns
OE# Valid to Output Delay, t_{GLQV} (max)	40 ns	35 ns	40 ns	40 ns	35 ns
OE# High to Data Invalid, t_{OH} (min)(4)	0	0	0	0	0
OE# High to Data Float, t_{GHQZ} (max)(4)	25 ns	25 ns	20 ns	20 ns	20 ns

Table 2. Read Timing Parameters (V_{CC} = 5V ± 5%)(2)

Timing Description	28F800BV-120	28F800BV-70 28F800B5-70	28F400BV-120	28F400BV-80 28F400B5-80	28F400BV-60 28F400B5-60
Address Valid to Data Valid, t_{AVQV} (max)	120 ns	70 ns	120 ns	80 ns	60 ns
CE# Valid to Data Valid, t_{ELQV} (max)	120 ns	70 ns	120 ns	80 ns	60 ns
OE# Valid to Output Delay, t_{GLQV} (max)	40 ns	30 ns	40 ns	40 ns	30 ns
OE# High to Data Invalid, t_{OH} (min)(4)	0	0	0	0	0
OE# High to Data Float, t_{GHQZ} (max)(4)	20 ns	20 ns	20 ns	20 ns	20 ns

Table 3. Read Timing Parameters (V_{CC} = 3.3V ± 10%)(3)

Timing Description	28F800BV-120	28F800BV-70 28F800B5-70	28F400BV-120	28F400BV-80 28F400B5-80	28F400BV-60 28F400B5-60
Address Valid to Data Valid, t_{AVQV} (max)	150 ns	120 ns	180 ns	150 ns	110 ns
CE# Valid to Data Valid, t_{ELQV} (max)	150 ns	120 ns	180 ns	150 ns	110 ns
OE# Valid to Output Delay, t_{GLQV} (max)	90 ns	65 ns	90 ns	90 ns	65 ns
OE# High to Data Invalid, t_{OH} (min)(4)	0	0	0	0	0
OE# High to Data Float, t_{GHQZ} (max)(4)	55 ns	45 ns	25 ns	25 ns	25 ns

Table 4. Write Timing Parameters (V_{CC} = 5V ± 10%, V_{CC} = 5V ± 5%)(5,6)

Timing Description	28F800BV-120	28F800BV-70 28F800B5-70	28F400BV-120	28F400BV-80 28F400B5-80	28F400BV-60 28F400B5-60
Address Valid to WE# High, t_{AVWH} (min)	50 ns	50 ns	50 ns	50 ns	50 ns
Data Valid to WE# High, t_{DVWH} (min)	50 ns	50 ns	50 ns	50 ns	50 ns
WE# Pulse Width, t_{WLWH} (min)	50 ns	50 ns	50 ns	50 ns	50 ns
Address Hold from WE# High, t_{WHAX} (min)	0	0	0	0	0

Table 5. Write Timing Parameters (V_{CC} = 3.3V ± 10%)(3,6)

Timing Description	28F800BV-120	28F800BV-70 28F800B5-70	28F400BV-120	28F400BV-80 28F400B5-80	28F400BV-60 28F400B5-60
Address Valid to WE# High, t_{AVWH} (min)	150 ns	90 ns	150 ns	120 ns	90 ns
Data Valid to WE# High, t_{DVWH} (min)	150 ns	90 ns	150 ns	120 ns	90 ns
WE# Pulse Width, t_{WLWH} (min)	150 ns	90 ns	150 ns	120 ns	90 ns
Address Hold from WE# High, t_{WHAX} (min)	0	0	0	0	0

NOTES:

1. The read timings provided in Table 1 were taken from the respective component's datasheet and assume a commercial temperature range, 100 pF test load, and V_{CC} of 5V ± 10%.
2. The read timings provided in Table 2 were taken from the respective component's datasheet and assume a commercial temperature range, 30 pF test load, and V_{CC} of 5V ± 5%.
3. The read and write timings provided in Tables 3 and 5 were taken from the respective component's datasheet and assume a commercial temperature range, 50 pF test load, and V_{CC} of 3.3V ± 10%.
4. Data hold times and data float times assume that OE# rises before CE#.
5. The write timings provided in Table 4 were taken from the respective component's datasheet and assume a commercial temperature range. These specification are valid for a 100 pF test load and V_{CC} of 5V ± 10%, or for a 30 pF test load and V_{CC} of 5V ± 5%.
6. The write timing parameters assume WE#-controlled writes.

3.0 80186EB/EC BUS SIGNALS

A successful bus transfer relies on the timing of address, data, and control signals from the CPU. This section of the application note defines the essential signals used in an 80186EB/EC bus transfer.

3.1 Upper Address Bits

The upper bits of the address bus (A[19:16]) are multiplexed with bus status signals. During the address phase of a bus cycle, the upper four bits of the address are presented and can be latched using ALE. During other phases of a bus cycle, these signals represent bus status signals.

3.2 Address/Data Bus

The Address/Data Bus (AD[15:0]) provides multiplexed address and data access. During the address phase of the bus cycle, address bits 15 through 0 are presented on the bus and can be latched using ALE. Data information is transferred during the data acquisition phase of the bus cycle.

3.3 Address Latch Enable

The address latch enable signal (ALE) is used to strobe the address information to a latch during the address phase of the bus cycle. The address information must be latched with the falling edge of ALE before the multiplexed bus is used to transfer data or indicate other signals.

3.4 Read Indicator

The read strobe signal (RD#) indicates to an external memory device that it should drive data information onto the data bus. It is asserted during a read cycle following the address phase of the bus cycle.

3.5 Write Indicator

During a write cycle, the write strobe signal (WR#) indicates to an external memory device that data on the data bus is available to be accessed for a write. It is asserted during a write cycle following the address phase of the bus cycle.

3.6 Chip Select

Ten programmable chip select signals are available to enable external memory devices. There are eight general purpose chip selects (GCS[7:0]#) which are asserted whenever the address of a bus cycle is within the address limitations programmed by the user. The lower chip select (LCS#) is asserted whenever the address of a bus cycle is lower than the address limit specified by the user. The upper chip select (UCS#) is asserted whenever the address of a bus cycle is above the specified address limit. Only UCS# is active upon reset, so it must be used to select the boot device. For the analysis that follows, the chip select signals are collectively referenced by the signal name CS#.

3.7 Data Transceiver Enable

The data transceiver enable signal (DEN#) may be used to activate a bi-directional transceiver in a buffered system. It is used to avoid bus contention on the multiplexed address and data bus driven by the CPU and an external memory device.

3.8 Data Transfer Direction

The data transmit/receive signal (DT/R#) indicates the direction of data transfer during a bus cycle. The signal remains high during a write cycle and is lowered during a read cycle. It may be used in conjunction with DEN# to control the direction of data flow through a bi-directional transceiver in a buffered system.

4.0 READ TIMING ANALYSIS

This section discusses the key timing issues involved with the 80186EB/EC read cycle. Complete timing diagrams which include all essential microprocessor and flash device signals are shown in Figures 3 and 4 in Section 8.0.

4.1 Data Read Hold Time

The CPU requires that the data on the address/data bus remain valid for 3 ns after the falling edge of the clock at the end of the third clock cycle (T3). The CPU may negate RD# at the same time as this clock transition. If the output enable signal of the flash is triggered from the RD# signal, the data hold time requirement is violated because the data hold time for a 28Fx00B5/BV component is 0.

To solve this problem, DEN# in combination with DT/R# may be used to trigger the OE# signal of the flash device. The CPU negates DEN# a minimum of 3 ns after the falling edge of the clock at the end of T3. This delay meets the data hold time requirement of 3 ns.

4.2 Bus Contention

When using a multiplexed address and data bus, the problem of bus contention can arise during a read cycle. System errors or possible damage to a device may occur if two or more devices drive the bus at the same time. The two instances in the read cycle when a possible bus contention can occur are the transition from the address phase to the data acquisition phase and the transition from the data acquisition phase of one cycle to the address phase of the next cycle. The CPU must release its address signals to a high impedance state before the flash device drives data onto the bus. Likewise, the flash device must release its data signals to a high impedance state at the end of a bus cycle before the CPU drives the address onto the bus for the next cycle.

4.2.1 ADDRESS FLOAT TIME

During the first half of the second clock cycle (T2), the CPU releases the address/data bus by allowing the address signals to float to a high impedance state. At the same time, the CPU asserts the RD# signal to indicate to the flash device that it is ready to receive data. The RD# signal can occur almost one-half clock cycle before the address signals have been released. Since a 28Fx00B5/BV component may drive the bus immediately after receiving an enable signal, a bus

contention problem can occur if the OE# signal of the flash device is driven by the RD# signal of the CPU.

If OE# is triggered from DEN# in conjunction with DT/R#, as discussed in Section 4.1, the bus contention problem is avoided. The CPU asserts DEN# one-half clock cycle after the address signals are allowed to float to a high impedance state. This provides enough time for the CPU to release the bus before the flash device begins to drive data onto the bus.

4.2.2 DATA FLOAT TIME

The CPU requires that the address/data bus be in a high impedance state a minimum of one clock period minus 15 ns from the negation of RD#. The maximum data float time (t_{GHQZ}) of 28Fx00B5/BV components meets this requirement for lower frequencies, but violates it for higher frequencies. To solve this problem a bi-directional buffer can be used for the address/data bus. The buffer is enabled by DEN#, and the data transfer direction is controlled by DT/R#. The buffer allows the address/data bus of the CPU to float to a high impedance state before the flash device has released it. The buffer is only needed for higher frequency operations. Refer to Tables 11 and 12 in Section 6.0 to determine if the buffer is necessary for a particular application.

4.3 Data Read Setup Time

The CPU requires that the data on the address/data bus be valid a minimum of t_{CLIS} prior to the falling edge of the clock at the end of the third clock cycle (T3). Assuming that DEN# is used to control OE# as required in Sections 4.1 and 4.2.1, the maximum time from the rising edge of the clock in T2 to valid data appearing on the data bus is determined by the sum of DEN# assertion delay (t_{CHOV}) and data access time from OE# (t_{GLQV}). The sum of these delays plus the required setup time must be less than or equal to one and one-half clock cycles for the transfer to be successful with no wait-states. Additional wait-states may be added if the access time is too slow.

4.4 System Reset

After the external RESIN# signal is raised to a high level, the CPU waits 7 clock cycles before the first instruction is fetched from address 0FFFF0H. Upon reset the CPU's UCS# registers are configured for the maximum 3 wait-states which provides a total of 6 additional clock cycles (minus required data setup time) before valid data is required on the address/data bus. The output delay from reset (t_{PHQV}) of a 28Fx00B5/BV component meets the reset requirements of the CPU for all frequencies at 5V operation.

The requirements are also met at 3V operation except at some of the higher frequencies. To correct the reset problem at higher frequencies, an RC circuit must be used to hold low the RESIN# pin of the CPU for a longer period of time than the RP# pin of the flash device is held low. The RC time constants required for specified operating conditions are shown in Table 6. The RC circuit is necessary only for the cases shown in Table 6 and only if the flash device is used as the boot device.

4.5 Memory Requirements

Table 7 indicates the read timing parameters required of a flash device to operate with zero wait-states and without an address/data bus buffer. Table 8 indicates which 28Fx00B5/BV components meet these requirements. Additional wait-states do not affect the requirement for t_{GHQZ}, which is the frequency limiting timing parameter.

The addition of an address/data bus buffer eliminates all dependence on the t_{GHQZ} parameter. Operation at a given frequency is then limited by the other requirements shown in Table 7. One additional wait-state in conjunction with the use of the buffer results in all 28Fx00B5/BV components meeting the timing requirements for all frequencies shown.

Table 6. RC Time Constant Required for Reset Circuit

V_{CC}	Frequency	Flash Component	t_{PHQV} (max)	CPU Reset Time (min)	RC Time Constant (min)
3.3V ± 10%	16 MHz	28F400B5/BV	0.80 µs	0.79 µs	0.01 µs
3.3V ± 10%	16 MHz	28F800B5/BV	0.80 µs	0.79 µs	0.01 µs
other			none		

Table 7. Read Timing Parameter Requirements (ns)(1)

V_{CC}	Timing Parameter(4)	8 MHz	13 MHz	16 MHz	20 MHz(3)	25 MHz(3)
5V ± 10%(5)	t_{AVQV} (max)	335	190	150	113	90
5V ± 10%(5)	t_{ELQV} (max)	335	190	150	113	90
5V ± 10%(5)	t_{GLQV} (max)	152	80	61	43	33
5V ± 10%(5)	t_{OH} (min)	0	0	0	0	0
5V ± 10%(5)	t_{GHQZ} (max)(2)	83	34	23	11	6
3.3V ± 10%	t_{AVQV} (max)	315	173	138		
3.3V ± 10%	t_{ELQV} (max)	315	176	140		
3.3V ± 10%	t_{GLQV} (max)	132	63	48		
3.3V ± 10%	t_{OH} (min)	0	0	0		
3.3V ± 10%	t_{GHQZ} (max)(2)	78	27	15		

Table 8. 28Fx00B5/BV Components Meeting Read Timing Requirements(1,6)

V_{CC}	Timing Parameter(4)	8 MHz	13 MHz	16 MHz	20 MHz(3)	25 MHz(3)
5V ± 10%(5)	t_{AVQV} (max)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	B, D, E	B, D, E
5V ± 10%(5)	t_{ELQV} (max)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	B, D, E	B, D, E
5V ± 10%	t_{GLQV} (max)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	
5V ± 5%	t_{GLQV} (max)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	B, E
5V ± 10%(5)	t_{OH} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
5V ± 10%	t_{GHQZ} (max)(2)	A, B, C, D, E	A, B, C, D, E	C,D,E		
5V ± 5%	t_{GHQZ} (max)(2)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E		
3.3V ± 10%	t_{AVQV} (max)	A, B, C, D, E	A, B, D, E	B, E		
3.3V ± 10%	t_{ELQV} (max)	A, B, C, D, E	A, B, D, E	B, E		
3.3V ± 10%	t_{GLQV} (max)	A, B, C, D, E				
3.3V ± 10%	t_{OH} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E		
3.3V ± 10%	t_{GHQZ} (max)(2)	A, B, C, D, E	C,D,E			

NOTES:

1. Read timing parameter requirements are specified for an interface which controls OE# with DEN# and DT/R# as discussed in Sections 4.1 and 4.2.1. Timing parameters given assume zero propagation delay due to interface logic. Requirements are based on the timing parameters of the lowest frequency 80186EB/EC component that is capable of operating at the specified frequency. If both EB and EC parts are available for a particular frequency, the parameters giving the worse timing margin are chosen.
2. Specification for t_{GHQZ} is required only if no address/data bus buffer is used. If buffer is used, requirement is met by all 28Fx00B5/BV components for all frequencies shown.
3. 20 MHz and 25 MHz values are not shown for V_{CC} = 3.3V ± 10% because the maximum available frequency for the 80L186EB/EC is 16 MHz.
4. Values for t_{AVQV}, t_{ELQV}, and t_{GLQV} are for a bus transfer with no wait-states. One clock period is added to each of these values for each additional wait-state.
5. Specification is also valid for V_{CC} = 5V ± 5%.
6. A = 28F800BV-120, B = 28F800B5/BV-70, C = 28F400BV-120, D = 28F400B5/BV-80, and E = 28F400B5/BV-60.

5.0 WRITE TIMING ANALYSIS

This section discusses the key timing issues involved with the 80186EB/EC write cycle. A complete timing diagram which includes all essential microprocessor and flash device signals is shown in Figure 5 in Section 9.0.

5.1 Data Write Setup Time

The CPU places valid data on the data bus a maximum of t_{CLOV} after the falling edge of the clock at the beginning of the second clock cycle (T2). This data must be valid for a time t_{DVWH} prior to the negation of WE#, which may occur as early as 2 ns prior to the falling edge of the clock at the beginning of T4. Adding a wait-state increases the setup time by one clock period.

5.2 Write Address Hold Time

The address placed on the address bus by the CPU must be valid until the WE# signal of the flash device is negated. The CPU meets this requirement at any frequency within its specified operating limits.

5.3 WE# Pulse Width

The WE# signal must be held low for a minimum duration of t_{WLWH}. The 80C186EB/EC CPUs meet this requirement for all 28Fx00B5/BV components at all frequencies within their specified operating limits. The low-voltage 80L186EB/EC CPUs violate the write pulse width requirement at higher frequencies. Adding a wait-state increases the write pulse width by one clock period and eliminate the violation.

5.4 Memory Requirements

Table 9 indicates the write timing parameters required of a flash device to operate with zero wait-states. Table 10 indicates which 28Fx00B5/BV components meet these requirements. One additional wait-state results in all 28Fx00B5/BV components meeting the timing requirements for all frequencies shown.

6.0 MAXIMUM OPERABLE FREQUENCY

The maximum operable frequency of a system is determined from the analysis of read and write timing parameters discussed in Sections 4.0 and 5.0. Table 11 indicates the maximum operable frequency of a system using zero wait-states and using no address/data bus buffer. Additional wait-states does not affect the maximum operable frequency.

Table 12 indicates the maximum operable frequency of a system using zero wait-states and using the address/data bus buffer discussed in Section 4.2.2. One additional wait-state results in a system that can operate at the maximum CPU frequency for all 80186EB/EC CPUs using any 28Fx00B5/BV components.

Table 9. Write Timing Parameter Requirements (ns)(1)

V_{CC}	Timing Parameter(3)	8 MHz	13 MHz	16 MHz	20 MHz(2)	25 MHz(2)
5V ± 10%(4)	t_{AVWH} (min)	343	198	158	121	98
5V ± 10%(4)	t_{DVWH} (min)	218	121	96	71	58
5V ± 10%(4)	t_{WLWH} (min)	245	148	120	95	75
5V ± 10%(4)	t_{WHAX} (min)	110	61	47	35	25
3.3V ± 10%	t_{AVWH} (min)	338	191	151		
3.3V ± 10%	t_{DVWH} (min)	213	119	93		
3.3V ± 10%	t_{WLWH} (min)	245	148	120		
3.3V ± 10%	t_{WHAX} (min)	110	61	47		

Table 10. 28Fx00B5/BV Components Meeting Write Timing Requirements(1,5)

V_{CC}	Timing Parameter(3)	8 MHz	13 MHz	16 MHz	20 MHz(2)	25 MHz(2)
5V ± 10%(4)	t_{AVWH} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
5V ± 10%(4)	t_{DVWH} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
5V ± 10%(4)	t_{WLWH} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
5V ± 10%(4)	t_{WHAX} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
3.3V ± 10%	t_{AVWH} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E		
3.3V ± 10%	t_{DVWH} (min)	A, B, C, D, E	B, E	B, E		
3.3V ± 10%	t_{WLWH} (min)	A, B, C, D, E	B, D, E	B, D, E		
3.3V ± 10%	t_{WHAX} (min)	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E		

NOTES:

1. Write timing parameter requirements are specified for an interface which uses WR# to control WE#. Timing parameters given assume zero propagation delay due to interface logic. Requirements are based on the timing parameters of the lowest frequency 80186EB/EC component that is capable of operating at the specified frequency. If both EB and EC parts are available for a particular frequency, the parameters giving the worse timing margin are chosen.
2. 20 MHz and 25 MHz values are not shown for V_{CC} = 3.3V ± 10% because the maximum available frequency for the 80L186EB/EC is 16 MHz.
3. Values for t_{AVWH}, t_{DVWH}, and t_{WLWH} are for a bus transfer with no wait-states. One clock period is added to each of these values for each additional wait-state.
4. Specification is also valid for V_{CC} = 5V ± 5%.
5. A = 28F800BV-120, B = 28F800B5/BV-70, C = 28F400BV-120, D = 28F400B5/BV-80, and E = 28F400B5/BV-60.

Table 11. Maximum Operable Frequency (MHz) Without Address/Data Bus Buffer

V_{CC}	CPU	28Fx00BV-120	28F400BV-80	28F800BV-70	28F400BV-60
5V ± 10%	80C186EB-25	16.95	18.52	16.95	18.52
5V ± 10%	80C186EC-25	16.95	18.52	16.95	18.52
5V ± 10%	80C186EB-20	15.63	16.95	15.63	16.95
5V ± 10%	80C186EC-20	13.16	17.54	16.13	17.54
5V ± 10%	80C186EB-13	13.00	13.00	13.00	13.00
5V ± 10%	80C186EC-13	13.00	13.00	13.00	13.00
5V ± 5%	80C186EB-25	18.52	18.52	18.52	18.52
5V ± 5%	80C186EC-25	18.52	18.52	18.52	18.52
5V ± 5%	80C186EB-20	16.95	16.95	16.95	16.95
5V ± 5%	80C186EC-20	17.54	17.54	17.54	17.54
5V ± 5%	80C186EB-13	13.00	13.00	13.00	13.00
5V ± 5%	80C186EC-13	13.00	13.00	13.00	13.00
3.3V ± 10%	80L186EB-16	10.31	11.54	11.49	14.29
3.3V ± 10%	80L186EC-16	9.8	11.11	10.87	13.64
3.3V ± 10%	80L186EB-13	10.31	11.11	11.49	13.00
3.3V ± 10%	80L186EC-13	9.62	10.56	10.64	12.82
3.3V ± 10%	80L186EB-8	8.00	8.00	8.00	8.00

Table 12. Maximum Operable Frequency (MHz) with Address/Data Bus Buffer

V_{CC}	CPU	28F800BV-120	28F400BV-80	28F400BV-60
5V ± 10%	80C186EB-25	20.00	22.39	24.19
5V ± 10%	80C186EC-25	20.00	22.39	24.19
5V ± 10%	80C186EB-20	19.11	20.00	20.00
5V ± 10%	80C186EC-20	19.61	20.00	20.00
5V ± 10%	80C186EB-13	13.00	13.00	13.00
5V ± 10%	80C186EC-13	13.00	13.00	13.00
5V ± 5%	80C186EB-25	20.00	22.39	25.00
5V ± 5%	80C186EC-25	20.00	22.39	25.00
5V ± 5%	80C186EB-20	19.11	20.00	20.00
5V ± 5%	80C186EC-20	19.61	20.00	20.00
5V ± 5%	80C186EB-13	13.00	13.00	13.00
5V ± 5%	80C186EC-13	13.00	13.00	13.00
3.3V ± 10%	80L186EB-16	11.17	11.54	14.29
3.3V ± 10%	80L186EC-16	10.99	11.11	13.64
3.3V ± 10%	80L186EB-13	10.99	11.11	13.00
3.3V ± 10%	80L186EC-13	10.56	10.56	12.82
3.3V ± 10%	80L186EB-8	8.00	8.00	8.00

NOTE:

All specifications are for an interface which controls OE# with DEN# and DT/R# as discussed in Sections 4.1 and 4.2.1. Operating frequencies given assume zero propagation delay due to interface logic, zero wait-states, and proper reset circuitry for boot devices, if required, as discussed in Section 4.4.

7.0 INTERFACE LOGIC

This section of the application note describes the interface logic required when interfacing an 80186EB/EC embedded microprocessor to 28Fx00B5/BV flash components. The physical means of implementing the required logic is not specified. This decision is left to the system designer.

7.1 Address Latch

The address signals are time multiplexed with data and other signals. To hold the address valid on the address lines of the flash device, a transparent latch must be used to latch the address signals from the CPU during the address phase of a bus cycle. The enable signal to this latch is synchronized directly with ALE.

7.2 Enable Signals

The flash device responds to control signals placed on its CE#, OE#, and WE# enable lines. These signals must be synchronized with the CS#, RD#, WR#, DEN#, or DT/R# control signals from the CPU in such a way that no timing conflicts occur.

7.2.1 CE# AND WE# CONTROL

The CS# signal from the CPU is asserted when the address for a bus cycle is within a specified address range. This signal is not the time-limiting control signal in the bus cycle, so it may be connected directly to CE# without producing any timing conflicts.

The data on the address/data bus and the address from the transparent latch remain valid for a sufficient time after WR# is negated. Because of this adequate hold time, and because there is not a danger of bus contention during a write cycle, the WR# signal may be connected directly to WE# without producing any timing conflicts.

7.2.2 OE# CONTROL

As discussed in Sections 4.1 and 4.2.1, there are data hold and bus contention problems associated with the use of RD# to control OE#. The timing of DEN# provides better timing margins for these problems. To control OE#, DT/R# must be used in conjunction with DEN# to enable OE# during a read cycle only. OE# is enabled when both DEN# and DT/R# are low. This provides adequate data hold time and eliminates the first bus contention problem in the bus cycle.

7.3 Data Buffer

As discussed in Section 4.2.2, there is a bus contention problem during the transition between bus cycles at higher frequencies. This problem may be eliminated by using a bi-directional buffer to control the ability of the flash device to drive the address/data bus. This buffer is enabled with the DEN# signal and the direction is controlled by DT/R#. The buffer is only needed for higher frequency operations. Refer to Tables 11 and 12 to determine if the buffer is necessary for a particular application.

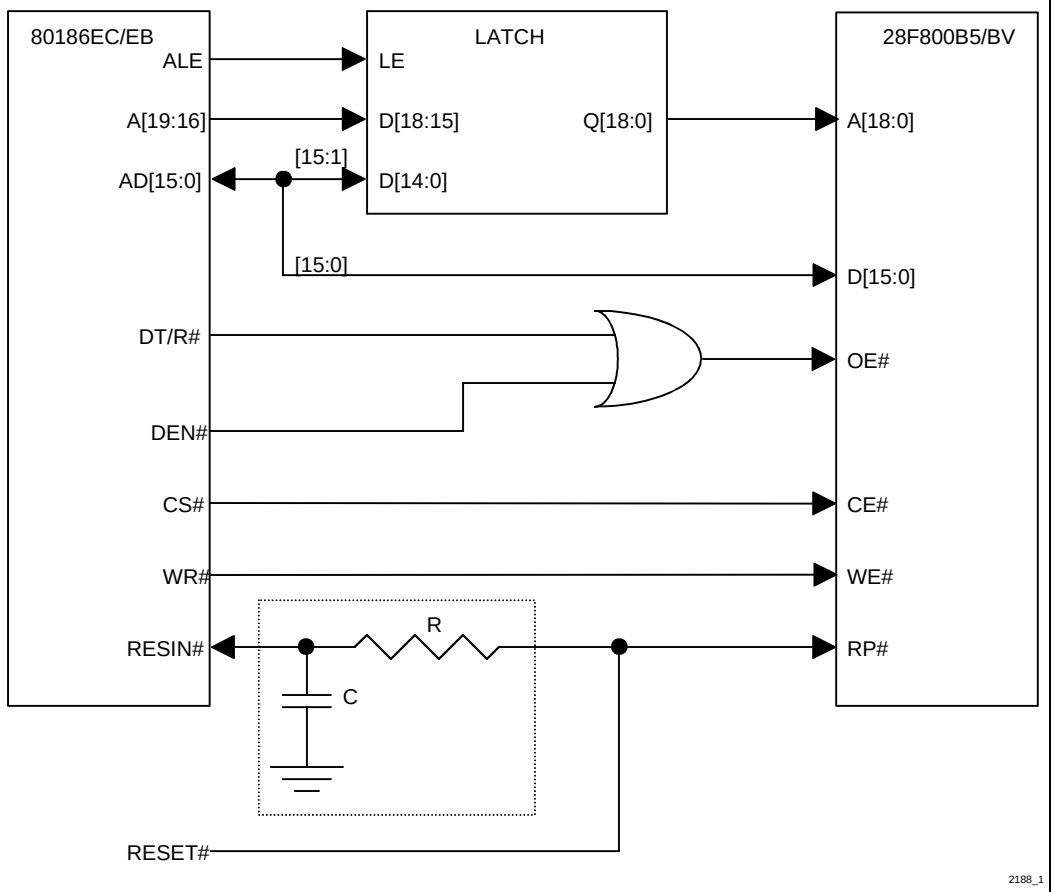
7.4 Reset Circuitry

At certain higher frequencies with a 3V power supply the flash device does not reset as fast as the CPU. To resolve this problem an RC circuit is used to hold low the RESIN# signal of the CPU for a longer period of time than the RP# signal of the flash device is held low. This RC circuit is only necessary for the operating conditions listed in Table 6 in Section 4.4 The required RC time constants for maximum CPU frequencies are also shown in Table 6. For all other operating conditions or if the flash device is not used as the system boot device, an external active low reset signal may be connected directly to both RESIN# and RP#.

7.5 Interface Diagrams

Figure 1 shows the logic that is necessary for the interface between the 80186EB/EC embedded microprocessor and a 28F800BV flash device. This diagram shows the interface that does not include the use of an address/data bus buffer. If a 28F400BV part is used, the most significant address bit from the CPU is not used and is not input to the latch. Figure 2 shows the same logic with the addition of a bi-directional buffer to control the access of the address/data bus. Refer to Tables 11 and 12 to determine if the buffer is required for a particular application.

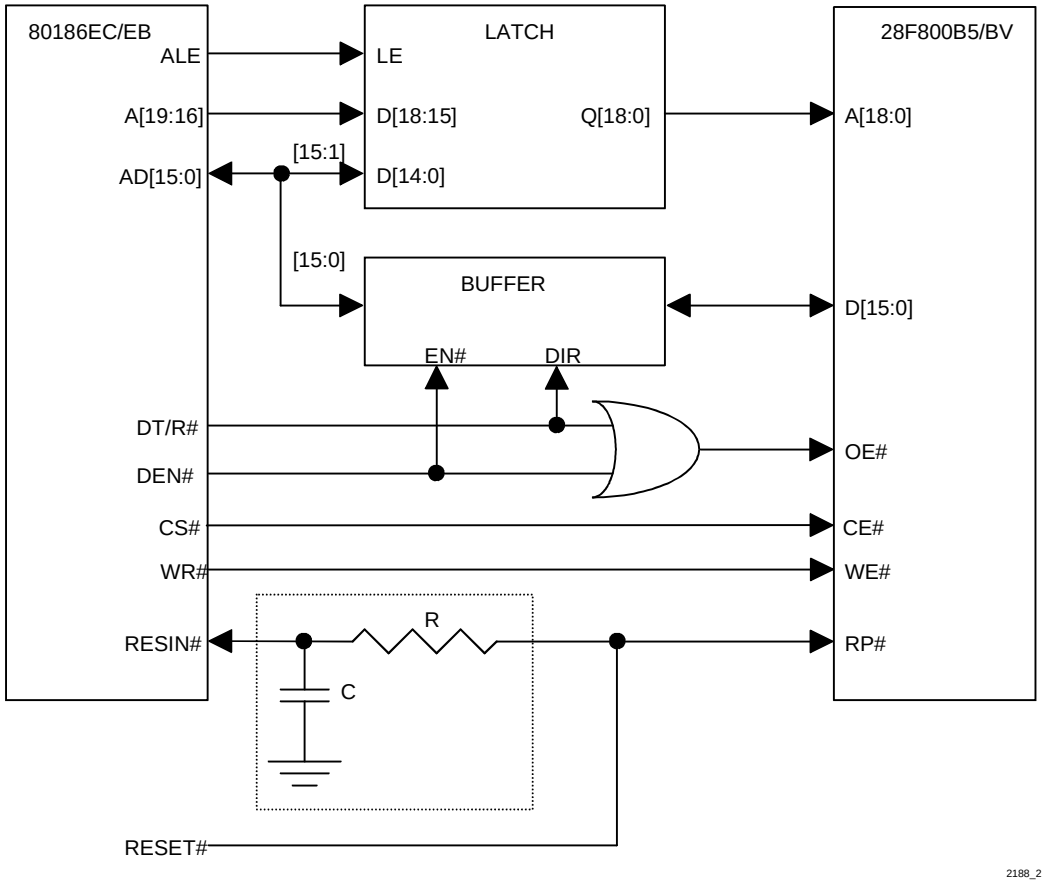
The reset RC circuit shown in both diagrams is enclosed in dashed lines to indicate that it is not required for all operating conditions. Refer to Table 6, in Section 4.4, to determine if the reset circuitry is required for a particular application.



NOTE:

Reset RC circuit shown in dashed lines is not needed for all operating conditions. Refer to Table6, in Section 4.4, to determine if the circuit is necessary for a particular application. Table 6 also gives RC time constants for maximum CPU frequencies. For interface to 28F400 components, the most significant address bit from the CPU is unused.

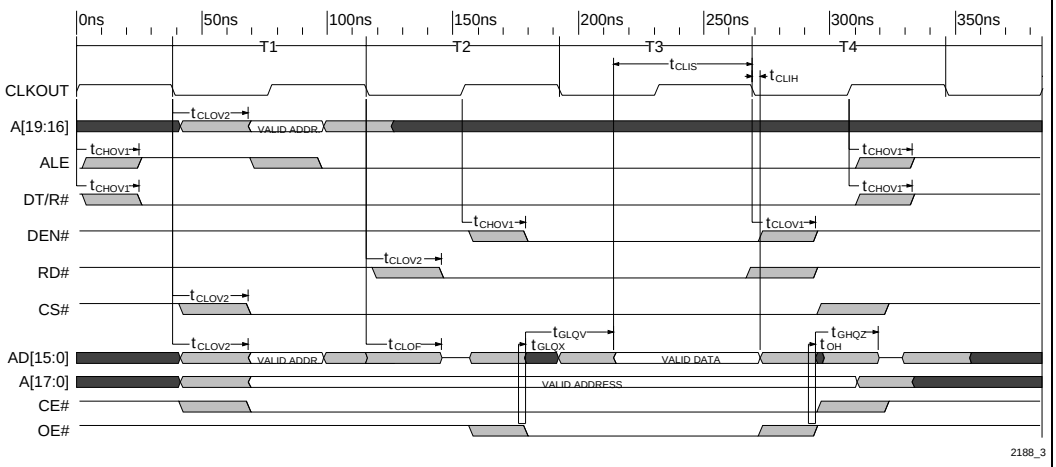
Figure 1. Interface Logic (Without Address/Data Bus Buffer)



NOTE:
Reset RC circuit shown in dashed lines is not needed for all operating conditions. Refer to Table6, in Section 4.4, to determine if the circuit is necessary for a particular application. Table 6 also gives RC time constants for maximum CPU frequencies. For interface to 28F400 components, the most significant address bit from the CPU is unused.

Figure 2. Interface Logic (with Address/Data Bus Buffer)

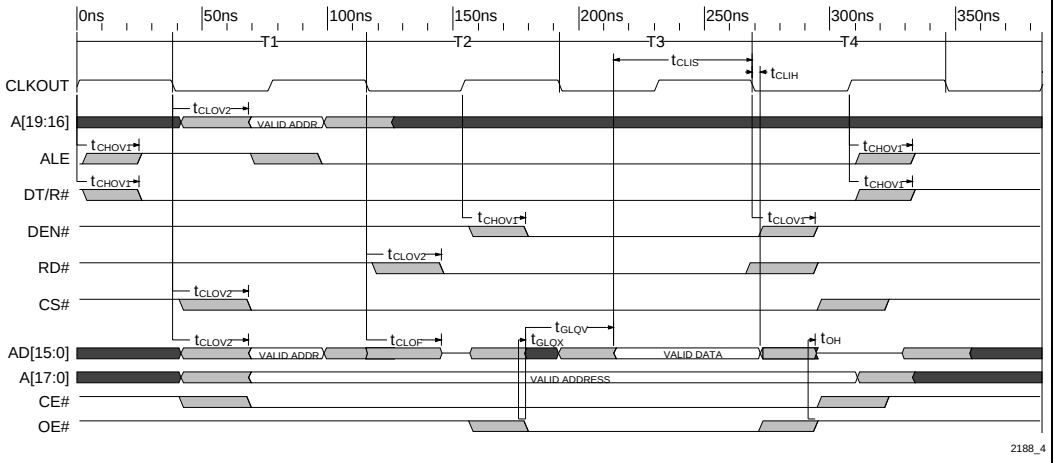
8.0 READ TIMING DIAGRAMS



NOTE:

Timing diagram uses timing parameters from an 80C186EC-13 and a 28F400B5/BV-60 with a 13 MHz clock and V_{CC} of 5V ± 10%. The numbering schemes for the naming of the t_{CLOVx} and t_{CHOVx} delays differ among the members of the 80186EB/EC family. Refer to respective datasheets for proper delay names.

Figure 3. Read Cycle (Without Address/Data Bus Buffer)

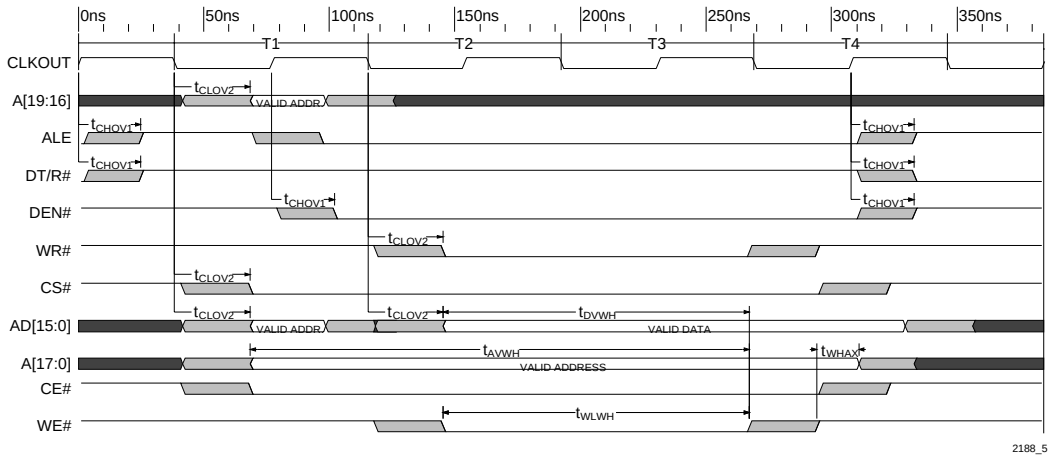


NOTE:

Timing diagram uses timing parameters from an 80C186EC-13 and a 28F400B5/BV-60 with a 13 MHz clock and V_{CC} of 5V ± 10%. The numbering schemes for the naming of the t_{CLOVx} and t_{CHOVx} delays differ among the members of the 80186EB/EC family. Refer to respective datasheets for proper delay names.

Figure 4. Read Cycle (with Address/Data Bus Buffer)

9.0 WRITE TIMING DIAGRAM



NOTE:

Timing diagram uses timing parameters from an 80C186EC-13 and a 28F400B5/BV-60 with a 13 MHz clock and V_{CC} of 5V ± 10%. The numbering schemes for the naming of the t_{CLOVx} and t_{CHOVx} delays differ among the members of the 80186EB/EC family. Refer to respective datasheets for proper delay names.

Figure 5. Write Cycle

APPENDIX A

ADDITIONAL INFORMATION(1,2)

Order Number	Title
272430	*80186/80188 High-Integration 16-Bit Microprocessors*
272433	*80C186EB/80C188EB and 80L186EB/80L188EB 16-Bit High-Integration Embedded Processors*
272434	*80C186EC/80C188EC and 80L186EC/80L188EC 16-Bit High-Integration Embedded Processor*
290599	*Smart 5 Boot Block Flash Memory Family 2, 4, 8 Mbit*
290539	*8-Mbit SmartVoltage Boot Block Flash Memory Family*
290530	*4-Mbit SmartVoltage Boot Block Flash Memory Family*
290531	*2-Mbit SmartVoltage Boot Block Flash Memory Family*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.