AP-393

APPLICATION NOTE

28F016SV Compatibility with 28F016SA

December 1996

Order Number: 292144-004

CONTENTS

REVISION HISTORY

Number	Description
-001	Original Version
-002	Added new RY/BY# mode of 28F016SV (Pulse-On-Write/Erase). Added/Revised DC/AC Characteristics based on 28F016SV Datasheet (Rev. 002) - Increased I_{CCR} Added to Tables 8 and 9. - Decreased I_{CCES}, I_{PPR}, I_{PPES} Added to Tables 8 and 9. - t_{PHOV} Added to Table 10. - t_{PHOV} and t_{GLQV} Added to Table 11. - t_{PHWL} Added to Table 12. - t_{PHEL}, t_{AVWH}, t_{DVWH}, t_{WLWH} and t_{PHWL} Added to Table 13. - t_{PHEL} Added to Table 14. - t_{PHWL}, t_{AVEH}, t_{DVEH}, t_{ELEH} and t_{PHEL} Added to Table 15. Tables 16 and 17 Consolidated into Tables 12 and 13. Added “Swap Page Buffer” to Pseudocode Example in Section 4.1.
-003	Added 3/5# pin to Figures 1 and 2; Updated Sections 1.0, 2.1 and 2.8 accordingly. Updated Tables 4–7 to reflect specifactions of latest datasheet revisions. Added “Erase Suspend Latency Time to Read” and “Auto Erase Suspend Latency Time to Write” Specifications to Tables 4–7. Increased I_{PPR} (V_{PP} Read Current) for $V_{PP} > V_{CC}$ to 200 µA at V_{CC} = 3.3V and V_{CC} = 5V Increased t_{PHQV} Specifications at 5V V_{CC} to 400 ns in Table 11. Updated Additional Information Section. Made minor cosmetic changes throughout document.
-004	Deleted AC/DC cycling tables

1.0 INTRODUCTION

This application note discusses compatibility between the 28F016SV and 28F016SA FlashFile™ memory components. It also offers recommendations for designing systems using the 28F016SA today, when future conversion to the 28F016SV is planned.

The 28F016SV is a member of Intel's second-generation 16-Mbit FlashFile component product family. It improves upon the 28F016SA in the following areas:

- SmartVoltage technology
  - — Selectable 5V or 12V V_{PP}
- Faster read performance
- Higher Page Buffer write performance at 12V V_{PP}
- Enhanced device feedback after writing the Upload Device Information command
- Additional RY/BY# configuration
  - — Pulse-On-Program/Erase

2.0 COMPATIBILITY

The 28F016SV and 28F016SA are both manufactured on Intel's fourth-generation 0.6 micron ETOX™ IV process technology. This technology enables random access flash memory products with the highest read/program performance and lowest power consumption. ETOX flash memory technology also achieves very high quality and reliability.

The following sections discuss specific areas of compatibility between the 28F016SV and the 28F016SA. Please reference the documentation listed in Appendix A for additional information.

2.1 Pinout and Package

The 28F016SV is fully pinout backwards-compatible with the 28F016SA (see the *Intel Flash Memory Databook*). Both devices are available in 56-lead TSOP and SSOP packages.

2.2 Bus Operations

The 28F016SV shares the same bus operations as the 28F016SA, and both flash memories operate identically in these operating modes. See the *Intel Flash Memory Databook* for a complete description of bus operations for the 28F016SV/SA

2.3 Command Definitions

The 28F016SV shares the same command set as the 28F016SA. All commands produce compatible, internal operations for both flash memories. See the *Intel Flash Memory Databook* for a complete description of command definitions for 28F016SV/SA.

The 28F016SV includes an additional RY/BY# mode, RY/BY# Pulse on Program/Erase, enabled as part of the RY/BY# Configuration (96H) command sequence. This mode was "reserved for future use" on the 28F016SA.

The 28F016SV also enhances the device feedback after writing the Upload Device Information (99H) command sequence. It outputs not only the Device Revision Number (compatible with the 28F016SA), but the Device Proliferation Code and Device Configuration Code. See the *Intel Flash Memory Databook* for more information on these topics.

2.4 Status Registers

The 28F016SV and 28F016SA both have a Compatible Status Register (CSR), Global Status Register (GSR) and 32 Block Status Registers (BSRs). Register address maps for both flash memories are identical.

Compatible Status Register

CSR bits 4–7 have identical functions for both the 28F016SV and the 28F016SA. CSR bits 0–2 are marked "reserved for future use" for both the 28F016SV and 28F016SA.

CSR bit 3 (V_{PP} Status) has been functionally enhanced on the 28F016SV, reflective of the ability to Data Program and Erase with V_{PP} = 5.0V ± 10% (V_{PPH1}) or V_{PP} = 12.0V ± 5% (V_{PPH2}). See the *Intel Flash Memory Databook* for more information on 28F016SV Data Program and Erase. CSR.3 = "1" is defined as "V_{PP} Error" on the 28F016SV, versus "V_{PP} Low" on the

28F016SA. If Data Program or Erase is initiated with V_{PP} = V_{PPH2}, subsequent V_{PP} transitions above V_{PPH2}(max) or below V_{PPH2}(min) will, if detected, terminate the operation in progress and set CSR.3 to "1" (this functionality matches the 28F016SA). Additionally, if Data Program or Erase is initiated with V_{PP} = V_{PPH1}, subsequent V_{PP} transitions above V_{PPH1}(max) or below V_{PPH1}(min) will, if detected, also terminate the operation in progress and set CSR.3 to "1." See the *Intel Flash Memory Databook* for the 28F016SV's Compatibile Status Register.

Global Status Register

All GSR bits have identical functions for both the 28F016SV and the 28F016SA.

Block Status Registers

BSR bits 3–7 have identical functions for both the 28F016SV and the 28F016SA. BSR bit 0 is marked "reserved for future use" for both the 28F016SV and the 28F016SA.

BSR bit 2 (V_{PP} Status) has been functionally enhanced on the 28F016SV compared to the 28F016SA. See the earlier description of CSR.3 for more information.

BSR bit 1, marked "reserved for future use" on the 28F016SA, is the V_{PP} Level bit on the 28F016SV. BSR.1 reflects the V_{PP} level applied to the 28F016SV (V_{PPH1} = "1," V_{PPH2} = "0"). See the *Intel Flash Memory Databook* for the 28F016SV's Block Status Register.

2.5 Other Voltage and Current Specifications

The 28F016SV's typical and maximum V_{CC} read and V_{CC} standby (CMOS levels) currents are both higher than those of the 28F016SA.

The 28F016SV adds the V_{PPH1} (V_{PP} = 5V) program/erase voltage specification and V_{CC} and V_{PP} program and erase current specifications at V_{PP} = V_{PPH1}. Program/erase current specifications at V_{PP} = V_{PPH2} (12V) match those of the 28F016SA. The 28F016SV also lowers the V_{PPL} specification from 6.5V to 1.5V (to allow SmartVoltage operation) and renames this specification as V_{PPLK}, to signify the change. The 28F016SV's V_{CC}/V_{PP} erase suspend currents and V_{PP} read current (V_{PP} > V_{CC}) are lower than those of the 28F016SA.

See the *Intel Flash Memory Databook* for specific DC Characteristics of the 28F016SV/SA.

2.6 Read Timing Specifications

The 28F016SV "bin 1"' significantly improves many read specifications compared to the 28F016SA. At 3.3V V_{CC}, read performance is almost 2x that of "bin 2." See the *Intel Flash Memory Databook* for specific AC Read timings for the 28F016SV/SA.

2.7 Write Timing Specifications

The 28F016SV write timing specifications have also been improved to keep read and write cycle times equivalent and to simplify system interface to the flash memory. See the *Intel Flash Memory Databook* for specific Write timings for the 28F016SV/SA.

3.0 HARDWARE DESIGN FOR FORWARDS-COMPATIBILITY

Manufacturers who wish to use the 28F016SA now, and move to the 28F016SV for program performance, integration or other reasons, should keep the following focus areas in mind when completing designs:

3.1 V_{CC} Voltage

As noted in Section 2.5, the 28F016SV's typical and maximum read/standby current and typical deep power-down current are higher than those of the 28F016SA. V_{CC} power supply selection should factor in these higher currents, as should system power consumption calculations. Decoupling and bypass capacitors can supply current for any of the 28F016SV V_{CC} deep power-down mode current "spikes" (V_{CC} = 3.3V) with no added burden on the power supply.

If conversion to the 28F016SV will also include changing the program/erase voltage to 5V from 12V, 5V power supply current calculations should include both the future additional program/erase current drawn by the 28F016SV's V_{CC} input (if V_{CC} = 5V) and the future current drawn by the 28F016SV's V_{PP} input (connected to 5V).

3.2 V_{PP} Voltage

Conversion to the 28F016SV may be driven by the desire to program/erase at 5V (thereby eliminating the need for a separate 12V regulator). Keep in mind that program/erase at 5V is lower performance than at 12V. Some flash memory applications (but not all) can tolerate this additional program/erase time. For these applications, a jumper on the system board that enables V_{PP} pin connection either to the output of a 12V converter (for the 28F016SA) or to the system 5V supply (for the 28F016SV) should be added. With the jumper connected to 5V, the 12V converter and associated circuitry can be removed to lower system component count.

Write Protection Via V_{PPLK}

Switching V_{PP} off during normal operation is one of several methods commonly used to prevent unwanted alteration (data program or erase) of flash memory data. Designs that use this technique should ensure that the V_{PP} voltage transitions to GND when "off." Some 12V converters drop V_{PP} to a diode drop below V_{CC} when they are placed in shutdown. This will block unwanted data program and erase on the 28F016SA but not on the 28F016SV, which has a 5V V_{PP} option. An external pulldown resistor will pull the converter output to GND, preventing data alteration on either the 28F016SA or the 28F016SV. Other write protection techniques (i.e., RP# and WP# control) should also be used for full flash memory data protection.

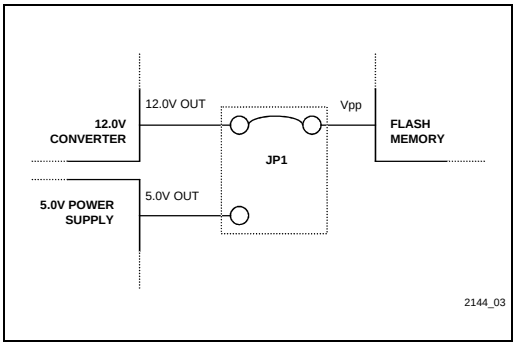

Figure 1. Jumper Selection of 12V Converter or 5V Power Supply Output for V_{PP}

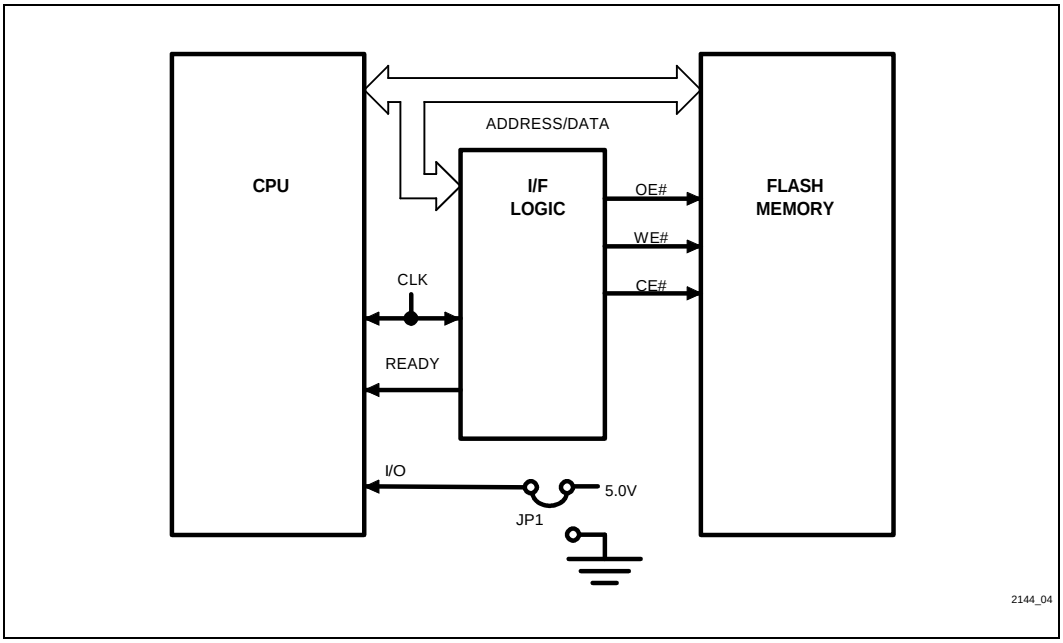

Figure 2. Jumper Identification of 28F016SA or 28F016SV Presence

3.3 Read/Program Performance and Wait-State Configuration

Conversion to the 28F016SV may also be driven by its higher read performance. Component identification in communicating whether the 28F016SA or the high-speed 28F016SV is in system can either be accomplished via hardware or software methods (see Sections 3.4 and 4.1). Depending which component resides in the system, the state machine within the interface logic and/or system software can modify the wait-state profile of the flash memory space to take advantage of the 28F016SV's higher read performance capability.

3.4 Hardware Identification of 28F016SA or 28F016SV

Jumpers can be used to communicate whether the 28F016SA or 28F016SV device is in the system. As the device identifiers for the 28F016SA and the 28F016SV are identical (see Section 4.1), software identification of one or the other flash memory via reading the device ID is not feasible. See Section 4.1 for a software method of identifying the 28F016SA or 28F016SV via the Device Proliferation Code. Jumper identification can also be used to enable system software usage of the 28F016SV's Status Register enhancements and Device Configuration Code. See Section 4 for more information

4.0 SOFTWARE DESIGN FOR FORWARDS-COMPATIBILITY

The 28F016SV is fully software backwards-compatible with the 28F016SA. This section discusses several 28F016SV enhancements that system software can access if desired. Keep in mind that these features are not available on the 28F016SA and their access and/or implementation should not be attempted when using the 28F016SA.

4.1 Software Identification of 28F016SA or 28F016SV

The 28F016SV's device identifier is identical to that for the 28F016SA. This enables all software written for the 28F016SA to be run on the 28F016SV unchanged. Methods of identifying the 28F016SV in the system, such as the jumper identification of Section 3.3, can be used in designs that can accept both the 28F016SV and the 28F016SA. An alternative software method uses the Device Proliferation Code, supported on the 28F016SV (01H), but not on the 28F016SA. By initializing the Page Buffer location corresponding to this code to a known value and then executing an Upload Device Information command sequence, subsequent reads of the Page Buffer will identify the specific FlashFile memory in the system. The Device Proliferation Code address in the Page Buffer is 1FH in x8 mode and 0FH (upper 8 bits) in x16 mode. A pseudocode flow for this technique is shown below:

Initialize Device Proliferation Code address in Page Buffer to 00H.
Execute Upload Device Information command sequence
Swap Page Buffer
Read from Device Proliferation Code address
    If data = 00H, 28F016SA is present
    If data = 01H, 28F016SV is present
End

4.2 Block Status Register V_{PP} Level Bit

Bit 1 of the Block Status Registers, a "reserved" bit on the 28F016SA, is the "V_{PP} Level" bit on the 28F016SV. System software interfacing to the 28F016SV can examine this bit and, by determining what V_{PP} voltage is in the system, gain an indication of the level of Data Program and Erase performance to be expected. This capability is particularly valuable when creating software that could run either in a 12V V_{PP} or 5V V_{PP} system (such as a low-level PCMCIA driver). Knowledge of Program/Erase performance allows software to adjust the frequency and duration of events such as background media cleanup to optimize system performance.

4.3 Enhanced V_{PP} Status Bit

Bit 2 of the Block Status Registers, functionally identical to bit 3 of the Compatible Status Register, is enhanced on the 28F016SV to reflect both 5V and 12V V_{PP} capability. With $V_{PP} = V_{PPH2}$ at the beginning of Data Program/Erase, V_{PP} transitions above V_{PPH2}(max) or below V_{PPH2}(min) will, if detected, terminate Data Program/Erase and return error indication via CSR.3 = BSR.2 ="1" (this is 100% compatible with the 28F016SA function). With $V_{PP} = V_{PPH1}$ at the beginning of Data Program/Erase, V_{PP} transitions above V_{PPH1}(max) or below V_{PPH2}(min) will, if detected, also terminate Data Program/Erase and return error indication via CSR.3 = BSR.2 = "1" (this is new to the 28F016SV). Accordingly, the CSR.3 = BSR.2 = "1" condition has been renamed from "V_{PP} Low" (the 28F016SA definition) to "V_{PP} Error."

4.4 RY/BY# Configuration

The 28F016SV adds the Device Configuration Code, accessible via the Page Buffer after first writing the Upload Device Information command sequence (see the *Intel Flash Memory Databook*). This code enables system software to read the currently-configured 28F016SV RY/BY# mode. The Device Configuration Code is located at Page Buffer address 1EH in x8 mode, 0FH (lower 8 bits in x16 mode).

As discussed earlier in Section 2.3, the 28F016SV includes an additional RY/BY# mode, RY/BY# Pulse on Program/Erase, enabled as part of the RY/BY# Configuration (96H) command sequence. This mode was "reserved for future use" on the 28F016SA.

5.0 CONCLUSION

This application note has summarized upgrade considerations and compatibility areas between the 28F016SA and the 28F016SV. Consult reference documentation for a more complete understanding of compatibility and device capabilities. Please contact your local Intel or distribution sales office for more information on Intel's Flash memory products.

APPENDIX A
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
290528	*28F016SV Datasheet*
290489	*28F016SA Datasheet*
297372	*16-Mbit Flash Product Family User's Manual*
292092	*AP-357 Power Supply Solutions for Flash Memory*
292123	*AP-374 Flash Memory Write Protection Techniques*
292126	*AP-377 16-Mbit Flash Product Family Software Drivers, 28F016SA/28F016SV/28F016XS/28F016XD*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
292165	*AB-62 Compiling Optimized Code for Flash Memories*
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016SV iBIS Models
Contact Intel/Distribution Sales Office	28F016SV VHDL Models
Contact Intel/Distribution Sales Office	28F016SV TimingDesigner* Library Files
Contact Intel/Distribution Sales Office	28F016SV Orcad and ViewLogic Schematic Symbols

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.