Low-Power Module SDRAM DIMM Routing Guidelines

Application Note

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Order Number: 273317-001

Application Note

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1.0 Introduction

The purpose of this application note is to define the routing guidelines for SDRAM DIMM memory systems in Low-Power Module/Intel® 440BX AGPset systems. The routing guidelines are specified in pre-layout simulation results only. Post-layout simulations and post-silicon signal integrity analysis are not available to correlate with pre-layout simulation results. When following these guidelines, it is recommended that the developer simulate these signals for proper signal integrity, flight time and cross talk.

Note: The guidelines in this application note are based on 100 MHz SDRAM DIMM designs; however, the same guidelines apply to 66 MHz SDRAM DIMM designs.

1.1 Key Terms

The Low-Power Module is designed for applied computing market segments. A complete description of the available modules is located in the *Intel® Pentium® II Processor with On-Die Cache – Low-Power Module* datasheet (order number 273257), the *Intel® Pentium® II Processor – Low-Power Module* datasheet (order number 273256), and the *Intel® Pentium® III Processor – Low-Power Module* datasheet (order number 273299).

Intel 440BX AGPset refers to both the 82443BX Host Bridge/Controller and the 82371EB PCI ISA IDE Xcelerator (PIIX4E). A complete description of the 82443BX is located in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet (order number 290633). The PIIIX4E is described in the *82371AB PCI ISA IDE Xcelerator (PIIX4)* datasheet (order number 290562).

SDRAM DIMM refers to synchronous DRAM dual in-line memory modules.

1.2 Related Documents

These documents are available for download from Intel's World Wide Web site at http://www.intel.com.

Table 1. Related Intel Documents

Document Title	Order Number
Intel® Pentium® III Processor – Low-Power Module datasheet	273299
Mobile Pentium® III Processor Specification Update	245306
Intel® Pentium® II Processor with On-Die Cache – Low-Power Module datasheet	273257
Intel® Pentium® II Processor – Low-Power Module datasheet	273256
Mobile Pentium® II Processor Specification Update	243887
Intel® 440BX AGPset: 82443BX Host Bridge/Controller datasheet	290633
82443BX Host Bridge/Controller Electrical and Thermal Specification datasheet addendum	273218
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Specification Update	290639
82371AB PCI ISA IDE Xcelerator (PIIX4) datasheet	290562
82371EB PCI ISA IDE Xcelerator (PIIX4E) Specification Update	290635

2.0 100-MHz SDRAM DIMM Memory Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. Even when these guidelines are followed, it is still highly recommended that the developer simulate these signals for proper signal integrity, flight time and cross talk.

2.1 100-MHz SDRAM DIMM Interface Overview

The 82443BX Host Bridge/Controller integrates a main memory DRAM controller that supports a 72-bit SDRAM array for 100-MHz environments. The DRAM controller interface is fully configurable through a set of control registers. A complete description of these registers is provided in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet (order number 290633).

2.1.1 SDRAM Interface Signals

A list of the signal names that are used in the 100-MHz SDRAM DIMM interface is provided in Table 2.

Note: MAB[13,10] are not inverted. These address bits are used to define various SDRAM commands.

Table 2. SDRAM Connectivity

82443BX Pins/Connection	DIMM Pins	Pin Function
CKBF buffer outputs DCLK[x:y]	CK[3:0] (4 DCLKs per DIMM)	Clock
CKE[3:0]	CKE[1:0]	Clock Enable
CSA3# CSA2# CSA1# CSA0#	S1, S3 (DIMM1) S0, S2 (DIMM1) S1, S3 (DIMM0) S0, S2 (DIMM0)	Chip Select
GND	A13	Address
MAB10, MAB#[9:0]	A[10:0]	Address
MAB#11	BA0	Address
MAB#12	BA1, A12	Address
MAB13	A11	Address
MD[63:0]	DQ[63:0]	Data
MECC[7:0]	CB[7:0]	Error Checking and Correction
Strap for SMBus Individual Address	SA[2:0]	SMBus Address
SMBDATA	SDA	SMBus Data
SMBCLK	SCL	SMBus Clock
SCASA#	CAS#	SDRAM Column Address Select
SRASA#	RAS#	SDRAM Row Address Select
WEA#	WE0#	Write Enable
DQMA[7:0]	DQM[7:0]	Input/Output Data Mask

NOTES:
1. Some of the pin ranges above are dependent on which DIMM is being reviewed; “x” and “y” indicate signal copies.
2. The memory data bit traces may be byte-swapped to simplify board routing and minimize trace lengths. This may also be done for the data bits within the byte channel.
3. System electronics board impedance should be 55 Ω ± 10%.
4. All resistors should be maximum 5% tolerance.
5. Populate the furthest DIMM first to avoid stub reflections.
6. See the *SDRAM Serial Presence Detect Data Structure* Specification for information on EEPROM register contents (http://developer.intel.com/design/chipsets/memory/spdsd12a.htm).

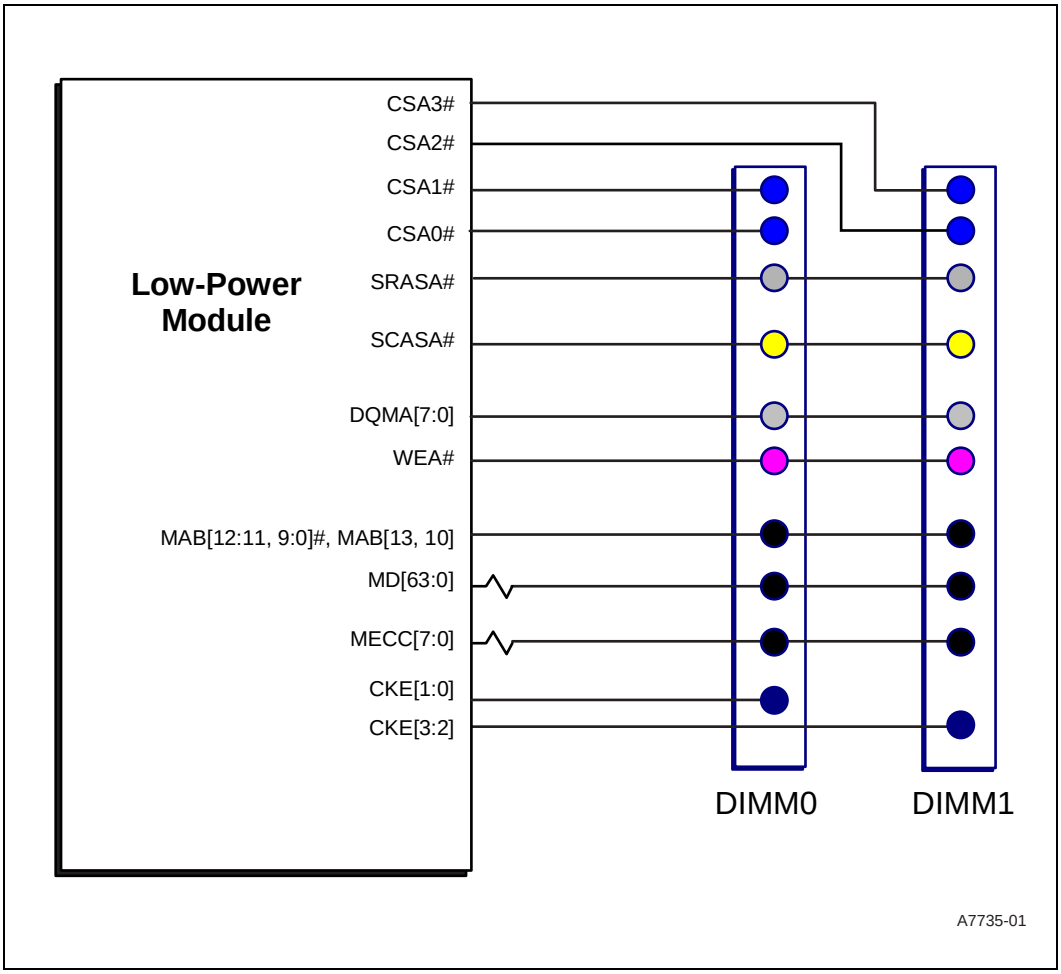
2.2 100-MHz SDRAM DIMM Layout Guidelines

This section explains the connectivity between the Low-Power Module and the 100-MHz SDRAM DIMMs.

2.2.1 DIMM Connection - SDRAM

Figure 1 shows the DIMM connections on the system electronics. The guidelines described in this document are based on the assumption that two DIMM slots are present on the system electronics.

Figure 1. SDRAM - Two DIMMs



2.2.2 Trace Lengths for Two DIMM Design

The following section illustrates signal topology and provides the minimum and maximum trace lengths to the DIMM connector pads for each signal group in a two-DIMM design.

2.2.2.1 Data - MD[63:0], MECC[7:0]

Figure 2. MD[63:0], MECC[7:0] Topology

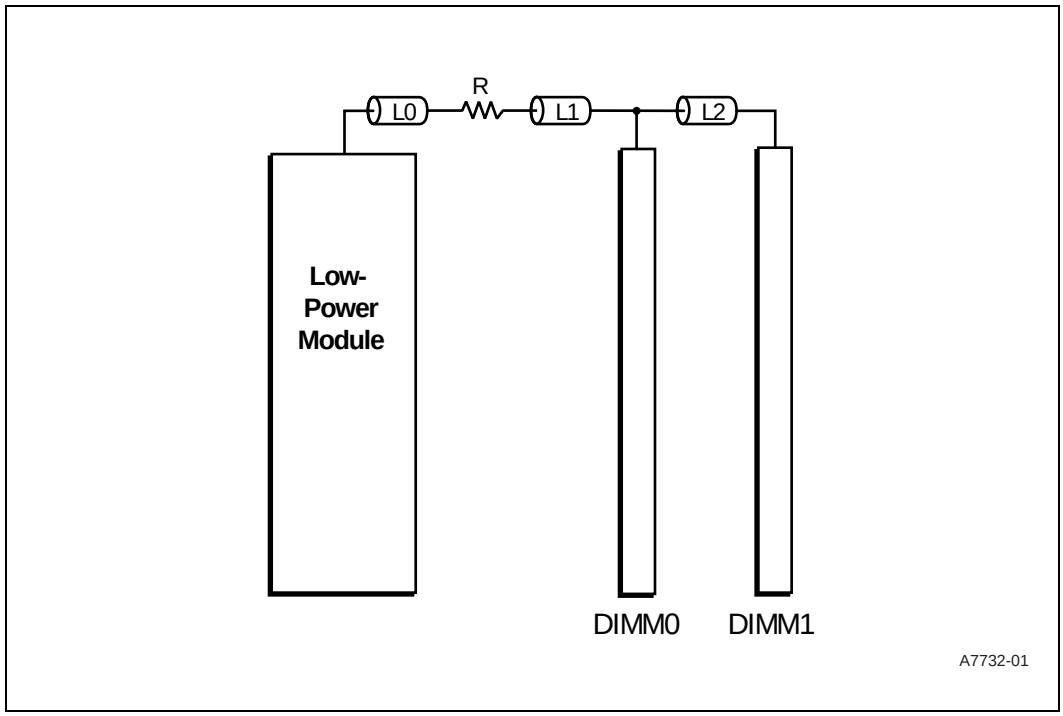


Table 3. Trace lengths MD[63:0], MECC[7:0]

Section	Minimum	Maximum
L0	0	1.0 in.
L2	0	0.6 in.
L0+L1	1.0 in.	< 4
L0+L1+L2	0	4.0 in.
Series R	n/a	10 Ω – 18 Ω ± 5%†

† Series termination values of 10 Ω for 100 MHz designs and 18 Ω for 66 MHz designs are based on simulation only and may not be required. Exact values should be determined through signal integrity validation.

Figure 3. DQMA[7:0] Topology

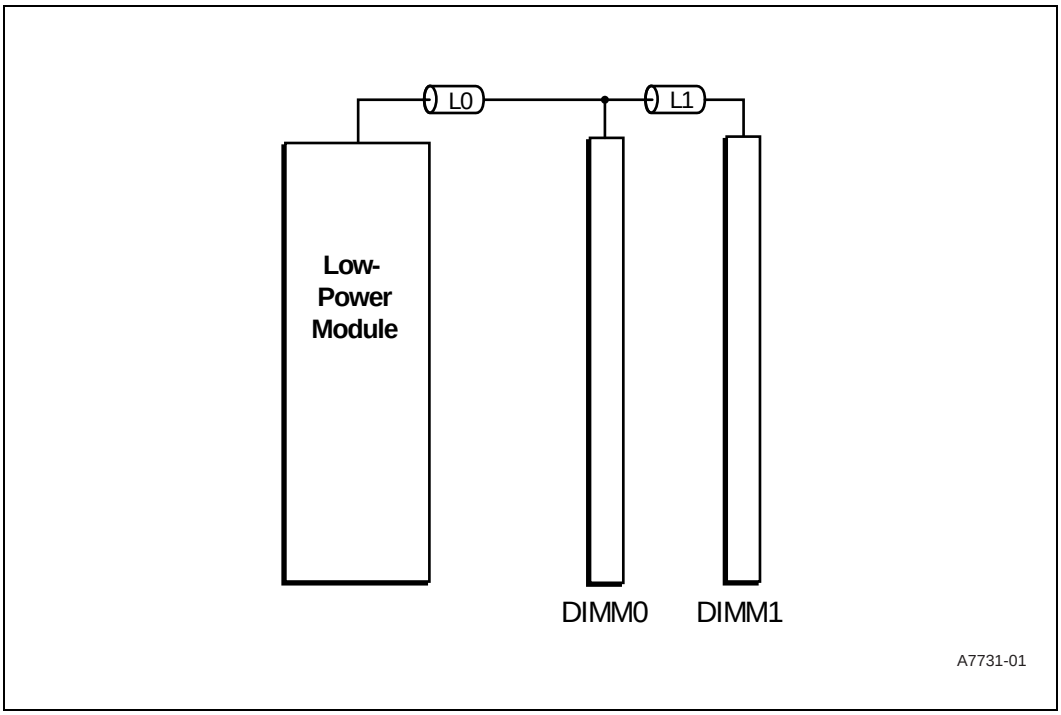


Table 4. Trace Lengths for DQMA[7:0]

Section	Minimum	Maximum
L0	1.0 in.	n/a
L1	n/a	1.0 in.
L0 + L1	n/a	4 in.

2.2.2.2 Chip Select - CSA[3:0]#

Figure 4. CSA[3:0]# Daisy Chain Topology

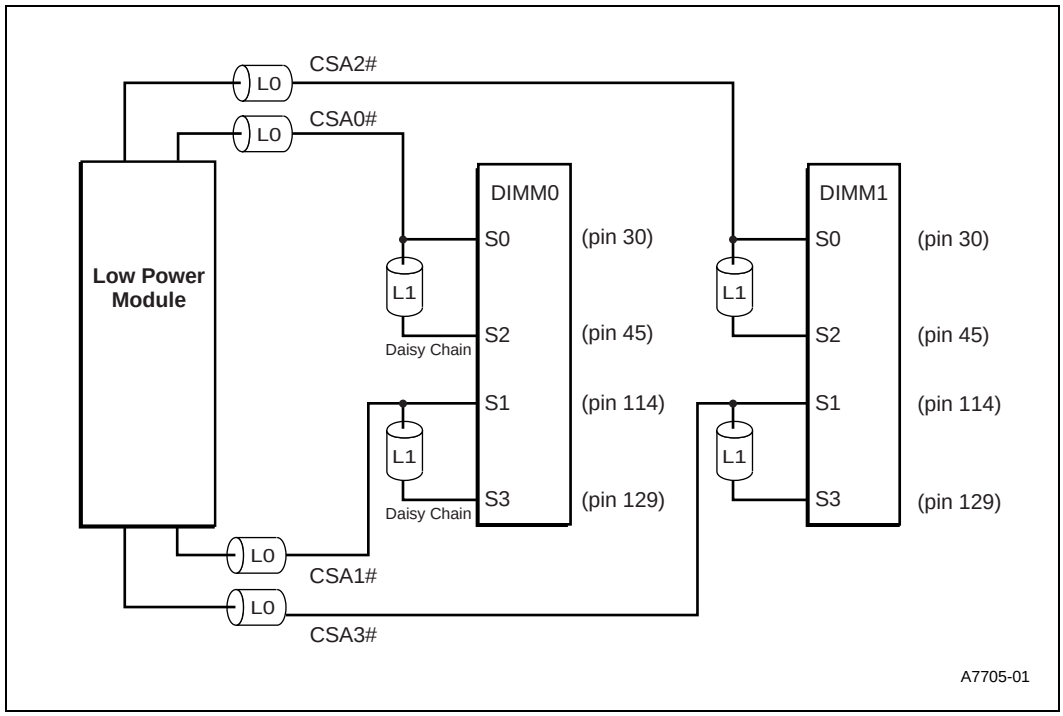


Table 5. Trace Lengths for CSA[3:0]#

Section	Minimum	Maximum
L0	1 in.	3 in.
L1	n/a	1.0 in.

Due to unbalanced loading, route Pin 30 (S0) first, then route Pin 45 (S2) for CSA0# on DIMM0. Route Pin 114 (S1) first, then route Pin 129 (S3) for CSA1# on DIMM0. Follow similar restrictions when routing DIMM1 signals.

Limit each CSA[3:0]# signal to only three vias. One at the module and one at each DIMM pin. CSA signals should never change reference planes from where they enter the FAB to where they connect to the DIMM pad. CSA signals should be routed on surface layers whenever possible.

2.2.2.3 Clock Enable - CKE[3:0]

Figure 5. CKE[3:0] Topology

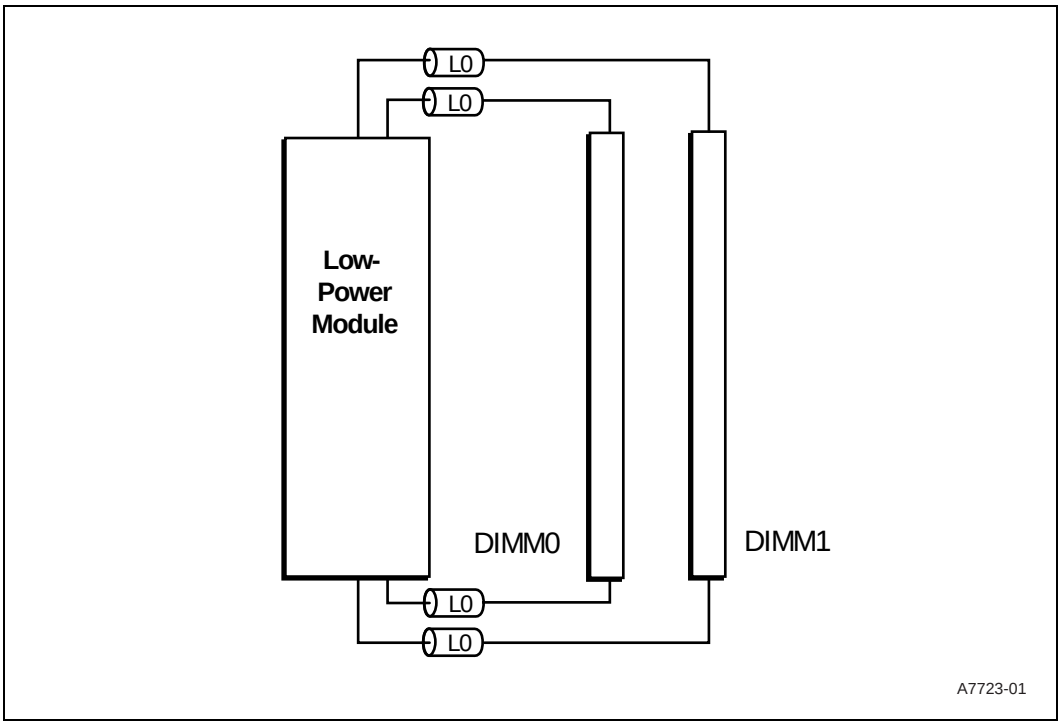


Table 6. Trace lengths for CKE[3:0]

Section	Minimum	Maximum
L0	1 in.	3.25 in.

2.2.2.4 Command - MAB[13:0]x, WEA#, SRASA#, SCASA#

Figure 6. MAB[13:0]x, WEA#, SRASA#, SCASA# Topology

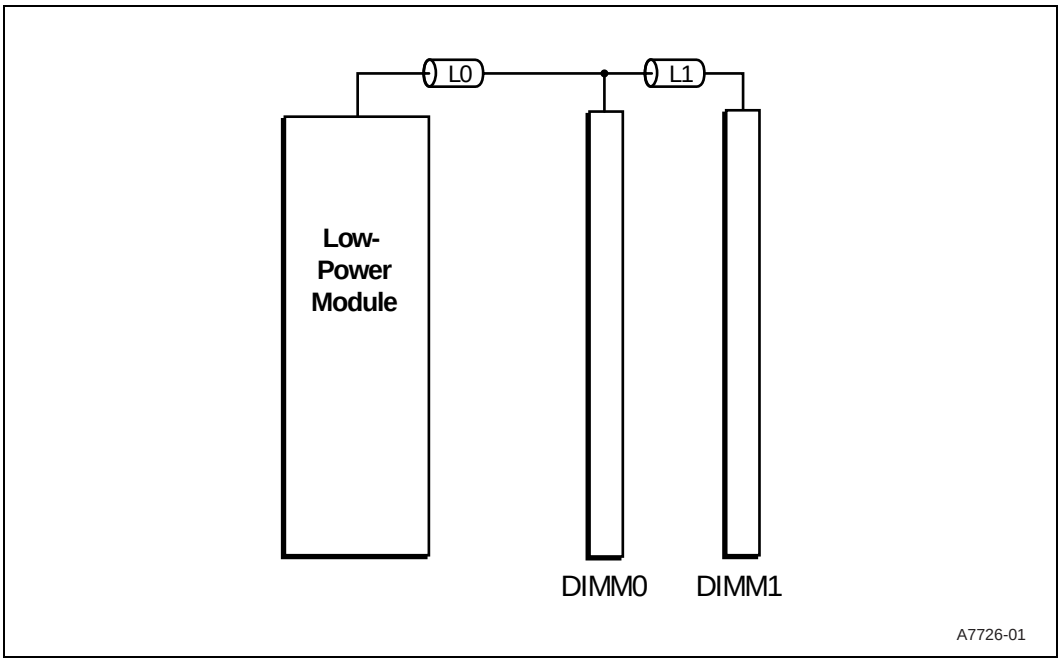


Table 7. Trace Lengths for MAB[13:0]x, WEA#, SRASA#, SCASA#

Section	Minimum	Maximum
L0	1.0 in.	n/a
L1	n/a	0.6 in.
L0 + L1	n/a	3.6 in.

3.0 SDRAM Clock Guidelines

This section defines the clock timing, lengths and series termination for SDRAM-related clocks.

3.1 Timing Guidelines

Figure 7 and Table 8 show a simplified SDRAM clock layout for the timing specifications.

Note: Even when following the SDRAM clock layout guidelines, it is highly recommended that the developer ensure that the maximum and minimum SDRAM clock skews are within the timing specifications.

Figure 7. SDRAM Clock Timing Specification

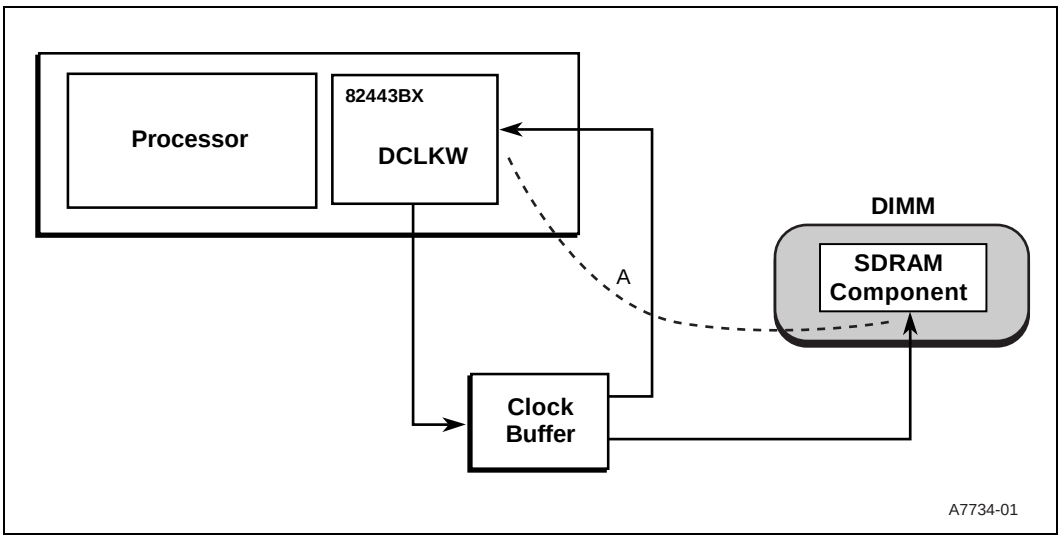


Table 8. Timing Specifications for Maximum and Minimum SDRAM Clock Skews

Symbol	Description	Ck100-M Pin-to-Pin	Boards	Total
A	DCLKWR to SDRAM (SCLK) skew	250 ps (max) -250 ps (min)	400 ps (max) -400 ps (min)	650 ps (max) -650 ps (min)

3.2 Clock Layout Guidelines

The following guidelines are required for proper clock layout:

- Series matching resistors are required.
  - — Place as near to the driver pin as possible (within 1 inch).
- Route all clocks on internal layers to provide better trace delay consistency and EMI containment.
- Set board impedance at 55 Ω ± 10%.
- Minimize the usage of vias in clock signals.
- Set the width to spacing ratio of all clocks to 1:2.
- All B1 trace lengths should be within 0.1” of each other.

Figure 8. Clocking Layout Diagram - 100 MHz

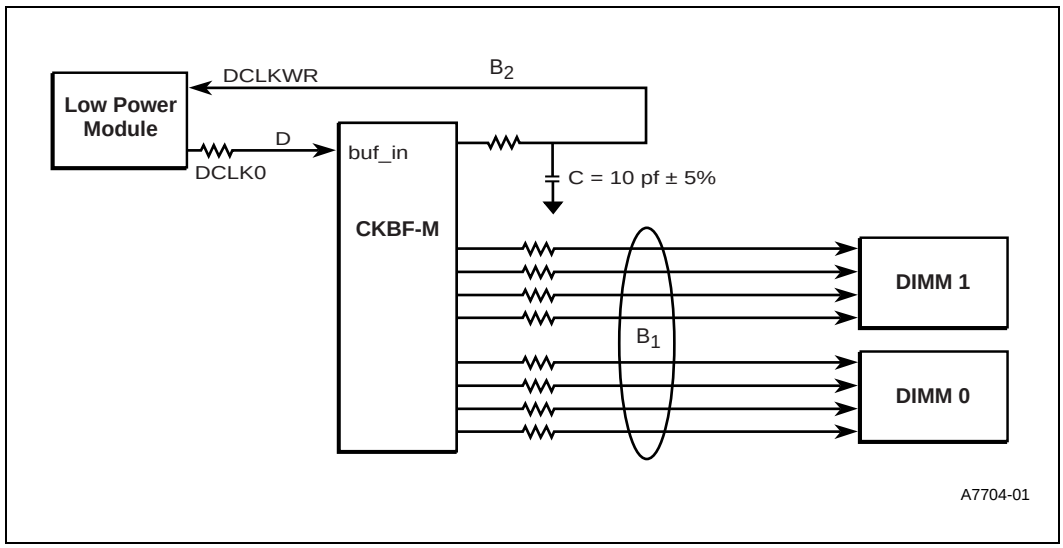


Table 9. Trace Lengths for SDRAM Clocks and DCLKWR

Variable	Trace Impedance	Trace Length	Minimum	Maximum	Resistor
D	55 Ω ± 10%	n/a	0 in.	4.0 in.	18 Ω ± 5%
B_1	55 Ω ± 10%	B	0 in.	3.0 in.	10 Ω ± 5%
B_2	55 Ω ± 10%	B + 4.8 in.	4.8 in.	7.8 in.	22 Ω ± 5%