AP-972

Application Note

Pentium® III Xeon™ Processor System Compatibility Guidelines

Order Number 245248-003

August, 2000

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked “reserved” or “undefined”. Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® Pentium® III Xeon™ processor may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Such errata are not covered by Intel's warranty. Current characterized errata are available on request.

THIS DOCUMENT IS PROVIDED “AS IS” WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein. Intel does not warrant or represent that such use will not infringe such rights.

*Third-party brands and names are the property of their respective owners.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling1-800-548-4725, or by visiting Intel's website at http://www.intel.com.

Table of Contents

1.0 Introduction

This document describes the main differences that exist between the Pentium® III Xeon™ processors with 1MB and 2MB L2 cache and previous generations of Pentium III Xeon processors. These guidelines are intended as a “checklist” to determine whether or not a system designed for previous SC330 processors will be able to support a Pentium III Xeon processor with 1MB and 2MB L2 cache or Pentium III Xeon processor with 256KB L2 cache, and as a summary of requirements for new platforms intending to support either of these processors. The information contained herein should be used in conjunction with specifications presented in the latest versions of the datasheets for the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache, as well as information provided in other Pentium III Xeon processor design guides. For the latest collection of collateral for the Pentium III Xeon processor family, visit Intel's web site at http://developer.intel.com/design/pentiumiii/xeon/.

The Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache use the same mechanical form factor and physical connector as previous Pentium II Xeon and Pentium III Xeon processors but add additional functionality including *On Cartridge Voltage Regulation (OCVR)*.

To determine whether or not the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache will operate reliably in a platform, a developer must ensure that the requirements in this guideline are fully satisfied. Intel strongly encourages complete signal integrity analysis and a careful examination of all signal timings. Some Pentium III Xeon processors with 1MB and 2MB L2 cache timing requirements and tolerances are more stringent than those found in previous processors. In addition the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache may require new thermal cooling solutions and new voltage and current delivery schemes.

2.0 Terminology

The following terms are used in this document and are defined here for clarification:

- **Pentium® III Xeon™ processor with 256KB L2 cache** - refers to a Pentium III Xeon processor which utilizes On Cartridge Voltage Regulator technology, or “OCVR”, and which has 256KB of Level 2 cache. The OCVR regulates VCC_CORE (the appropriate cartridge input voltage) to the required processor core voltage (VCC_CPU). The OCVR was developed to provide the necessary regulation to guarantee the highest possible frequency of operation for the Pentium III Xeon processor at 600 MHz and above.

- **Pentium® III Xeon™ processor with 1MB and 2MB L2 cache** - refers to a Pentium III Xeon processor which utilizes On Cartridge Voltage Regulator technology, or “OCVR”, and which has either 1MB or 2MB of Level 2 cache. The OCVR regulates VCC_CORE (the appropriate cartridge input voltage) to the required processor core voltage (VCC_CPU). The OCVR was developed to provide the necessary regulation to guarantee the highest possible frequency of operation for the Pentium III Xeon processor at frequencies of 600 MHz and above.

- **Pentium® III Xeon™ processor at 500 MHz and 550 MHz** - refers to a Pentium III Xeon processor without an OCVR, and requires separate VCC_CORE and L2 voltage sources.

- **Pentium® III Xeon™ processor** - refers to any Pentium III Xeon processor with 256KB L2 cache, Pentium III Xeon processor with 1MB and 2MB L2 cache, or Pentium III Xeon processor at 500 MHz and 550 MHz.

- **L2 cache** -The L2 cache is integrated directly on the processor core for the Pentium III Xeon processor with 256KB L2 cache and the Pentium III Xeon processor with 1MB and 2MB L2 cache, or is located on the substrate for the Pentium III Xeon processor at 500 MHz and 550 MHz.

- **2.8V Pentium® III Xeon™ processor** - refers to a Pentium III Xeon processor with 256KB L2 cache or a Pentium III Xeon processor with 1MB and 2MB L2 cache which can be powered with +2.8 volts applied to its VCC_CORE pins.

- **5/12V Pentium® III Xeon™ processor** - refers to a Pentium III Xeon processor with 256KB L2 cache or a Pentium III Xeon processor with 1MB and 2MB L2 cache which can be powered with either +5.0 or +12.0 volts applied to its VCC_CORE pins.

3.0 Upgradeability

Table 1: Pentium® III Xeon™ Processor System Level Compatibility.

System	Pentium III Xeon processor at 500 MHz and 550 MHz	Pentium III Xeon processor with 256KB L2 cache	Pentium III Xeon processor with 1MB and 2MB L2 cache
4-way systems based on Intel® 450NX PCIset and Profusion Chipsets	Supported	Not supported	Supported[1]
2-way systems based on Intel® 440GX AGPset	Supported	Not supported	Not supported
2-way systems based on Intel® 840 Chipset	Not supported	Supported at 133 MHz only	Not supported

1. To determine whether or not the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache will operate reliably in a platform, a developer has to ensure that the requirements listed in the appropriate processor datasheet and this document are fully satisfied.

4.0 Power and Thermal Requirements

Table 2 shows the power and Max T_{PLATE} requirements for SC330 processors that support 100 MHz system bus frequency. “FMB” stands for Flexible Mother Board and is a suggested design guideline for a flexible motherboard design targeted to allow forward compatibility with existing and future processors.

Table 2: Power & Thermal Requirements[1,2]

Processor	Processor Core Frequency	Thermal Plate Power	Max T_{PLATE}
Pentium® II Xeon™ processor	450 MHz	46.7 W	75° C
Pentium III Xeon processor	550 MHz	40.5 W	68° C
Pentium III Xeon processor with 256KB L2 cache	FMB	37.0 W	55° C
Pentium III Xeon processor with 1MB and 2MB L2 cache	FMB	50 W	65° C

1. Information in table is for reference only. Refer to the appropriate processor datasheet for valid and specifications.
2. Power and thermal numbers in this table are specific to each processor. Operating conditions for one processor type may not be applied to another processor type.

Table 3: Power and Thermal Solution Considerations

System Platform	Impact & Implications
Pentium® III Xeon™ processor with 256KB L2 cache systems with support for the Pentium III Xeon processor at 500 MHz and 550 MHz	System developers need to ensure the planned cooling solution can meet 68° C T_{PLATE} for the Pentium III Xeon processor at 500 MHz and 550 MHz, and 55° C T_{PLATE} for the Pentium III Xeon processor with 256KB L2 cache. The FMB ICC_CORE requirement for the 2.8V Pentium III Xeon processor with 256K L2 cache is a maximum of 16 A.
Pentium III Xeon processor with 256KB L2 cache systems without Pentium III Xeon processor at 500 MHz and 550 MHz support	System developers need to ensure the planned cooling solution can meet 55° C T_{PLATE} for the Pentium III Xeon processor with 256KB L2 cache. Developers will have the flexibility to create a Pentium III Xeon processor with 256KB L2 cache platform using 5V or 12V VCC_CORE supply, thus eliminating the need for a baseboard VCC_CORE VRM.
Pentium III Xeon processor with 1MB and 2MB L2 cache systems with support for the Pentium III Xeon processor at 500 MHz and 550 MHz	System developers need to ensure the planned cooling solution can meet 68° C T_{PLATE} for the Pentium III Xeon processor at 500 MHz and 550 MHz and 65° C T_{PLATE} for the Pentium III Xeon processor with 1MB and 2MB L2 cache.
Pentium III Xeon processor with 1MB and 2MB L2 cache systems without Pentium III Xeon processor at 500 MHz and 550 MHz support	System developers need to ensure the planned cooling solution can meet 65° C T_{PLATE} for the Pentium III Xeon processor with 1MB and 2MB L2 cache. Developers will have the flexibility to create a Pentium III Xeon processor with 1MB and 2MB L2 cache platform using 5V or 12V VCC_CORE supply, thus eliminating the need for a baseboard VCC_CORE VRM.

5.0 New ICCSMBus Specification

The Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache cartridge implement additional logic for OCVR control and miscellaneous logic. The ICC_{SMBus} specification changed from 10 mA on the Pentium II Xeon processor and Pentium III Xeon processor at 500 MHz and 550 MHz to 22.5 mA for the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache. Refer to the appropriate processor datasheet for details on this specification.

Table 4: ICC_{SMBus} Current Considerations.

System Design	Implications
Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache systems	System designers need to ensure ICCSMBus can supply at least 22.5 mA.

6.0 L2 Cache VID Settings

The Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache offer a processor core with integrated L2 cache, which eliminates the need for a VRM to power the L2 cache. To support platforms that intend to provide backward compatibility with the Pentium III Xeon processor at 500 MHz and 550 MHz, the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache implement the legacy VID pins for L2 cache, but with the lines encoded on the processor as “No Core”, VID_L2 [4:0] = 11111. When the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache are installed in these legacy platforms, the L2 VRMs are expected to disable themselves in response to this “No Core” VID setting as specified in legacy processor datasheet documentation. If Pentium III Xeon processor at 500 MHz and 550 MHz compatibility is not of concern, OEMs may decide to depopulate the L2 cache regulator or remove the entire VCC_L2 delivery on new designs since VCC_L2 is not required by the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache (the VCC_L2 pins are not connected inside these processor cartridges).

Table 5: L2 VID Setting Considerations.

System Design	Implications
• Pentium® III Xeon™ processor with 256KB L2 cache systems without Pentium III Xeon processor at 500 MHz and 550 MHz support • Pentium III Xeon processor with 1MB and 2MB L2 cache systems without Pentium III Xeon processor at 500 MHz and 550 MHz support	A separate L2 VRM and L2 VID setting scheme is not required since the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache have integrated L2 cache.
• Pentium III Xeon processor with 256KB L2 cache systems with Pentium III Xeon processor at 500 MHz and 550 MHz support • Pentium III Xeon processor with 1MB and 2MB L2 cache systems with Pentium III Xeon processor at 500 MHz and 550 MHz support	An L2 VRM is needed. The L2 VRM is expected to disable itself if a Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache is installed. System designers must ensure the baseboard is able to provide valid PWRGOOD and RESET# generation in spite of getting a "Not Present" VID_L2 from the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache cartridge. Baseboard developers need to accommodate the necessary logic to detect Pentium III Xeon processors at 500 MHz and 550 MHz and enable the L2 VRM.

7.0 Core Voltage Identification and HV_EN# Pin

The 2.8V Pentium® III Xeon™ processor uses the legacy VID scheme as per the *VRM 8.3 DC-DC Converter Design Guidelines* (please refer to the processor datasheet for further details). The expected operating voltage at the input of the OCVR for the 2.8V Pentium III Xeon processor is 2.8 V. Therefore, 2.8V Pentium III Xeon processor VID_CORE[4:0] inputs will encode the value for 2.8 V, VID[4:0] = 10111. The 5/12V Pentium III Xeon processor will encode the value for "No Core", VID[4:0] = 11111 since this processor type is meant to eliminate the need for VRMs.

To help identify 5/12V Pentium III Xeon processors, pin A3 (documented as an EMI pin for the Pentium III Xeon processor at 500 MHz and 550 MHz) is defined as the HV_EN# pin on the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache. HV_EN# is connected to GND inside the 5/12V Pentium III Xeon processor car-

tridges and left unconnected on 2.8V Pentium III Xeon processors and Pentium III Xeon at 500 MHz and 550 MHz processors. This allows baseboard logic to determine whether a high voltage (5V or 12V) can be applied to VCC_CORE pins, or whether the VCC_CORE must be provided through a VRM. Proper baseboard logic will:

1. Disable the processor VRM and apply 5V or 12V to VCC_CORE pins when a 5/12V Pentium III Xeon processor is installed. If 5/12V are not available, the system should disable the 5/12V Pentium III Xeon processor to prevent unexpected and unsupported operation.

2. Enable the processor VRM and apply the appropriate VRM voltage to the VCC_CORE pins when a Pentium III Xeon processor at 500 MHz and 550 MHz or 2.8V Pentium III Xeon processor is installed.

3. Disable 5/12V to VCC_CORE pins when a Pentium III Xeon processor at 500 MHz and 550 MHz or 2.8V Pentium III Xeon processor is installed to prevent damage and/or improper operation.

If the option of using pin A3 as an additional VID line is chosen the following table summarizes the VID coding presented by the processor cartridge and seen by the regulator (and any additional baseboard logic responsible for providing the correct voltage). VID[4:0] = 11111 is defined as “No Core” in the *VRM 8.3 DC-DC Converter Design Guidelines*.

Table 6: 2.8V and 5/12V Pentium® III Xeon™ Processor VID Settings[1,2,3]

Cartridge Version	HV_EN#	VID4	VID3	VID2	VID1	VID0
2.8 V	1	1	0	1	1	1
5 V and 12 V	0	1	1	1	1	1

1. Information in table is for reference only. Refer to the appropriate processor datasheet for valid specifications.
2. HV_EN# is not connected (floating) in 2.8V Pentium III Xeon processors.
3. “1” means the cartridge is not pulling this line low (i.e., floating).

If HV_EN# is used, the baseboard is responsible for ensuring no power sequencing problems (including power supply race conditions) occur between the VRM and the circuitry that bypasses either 5V or 12V.

Table 7: Core Voltage Identification and HV_EN# considerations

System Design	Implications
Systems with only VRM VCC_CORE supply (without 5/12V)	These designs will not be able to use the 5/12V Pentium® III Xeon™ processor. Power delivery solutions that do not use the VID scheme may be impacted Baseboard logic should: • Disable the 5/12V Pentium III Xeon processor to prevent unexpected operation and potential damage. • Enable the processor VRM and apply VRM voltage to VCC_CORE pins when a Pentium III Xeon processor at 500 MHz and 550 MHz or 2.8V Pentium III Xeon processor is installed.
Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache systems with both VRM and 5/12V VCC_CORE supplies	Baseboard logic should: • Disable the processor VRM and apply 5V or 12V to VCC_CORE when a 5/12V Pentium III Xeon processor is installed. • Disable the 5/12V supply to the VCC_CORE pins and enable the processor VRM (apply appropriate VCC_CORE voltage) when a 2.8V Pentium III Xeon processor or Pentium III Xeon processor at 500 MHz and 550 MHz is installed.

Table 7: Core Voltage Identification and HV_EN# considerations

System Design	Implications
Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache systems with only 5/12V VCC_CORE supply (no VRM)	Baseboard logic should: • Apply 5V or 12V to VCC_CORE when a 5/12V Pentium III Xeon processor is installed. • Disable the 5/12V supply to the VCC_CORE pins and disable a Pentium III Xeon processor at 500 MHz and 550 MHz or 2.8V Pentium III Xeon processor to prevent unexpected operation and potential damage.

8.0 SC330.1 Pin Changes over SC330 Definition

The SC330.1 definition is mechanically and electrically compatible with the SC330 definition. However, the new SC330.1 definition used by the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache redefine the following pins.

Table 8: SC330.1 Pin Changes[1]

Pin number	SC330 Name	SC330.1 Name	New Signal Buffer Type
A1	EMI	RESERVED_A1	Do not connect
A3	EMI	HV_EN#	Open or grounded on processor
A7	VSS	SELFSB1	CMOS Output
A9	SELFSB0	SELFSB0	CMOS Input
A11	TEST_VSS_A11	RESERVED_A11	Do not connect
A23	TEST_VCC_CORE_A23	TEST_2.5_A23	Pull up to 2.5V on baseboard
A26	RESERVED_A26	OCVR_EN	CMOS Input
B3	RESERVED _B3	OCVR_OK	Open Drain Output

Table 8: SC330.1 Pin Changes[1]

Pin number	SC330 Name	SC330.1 Name	New Signal Buffer Type
B27	TEST_VCC_CORE_B27	TEST_2.5_B27	Pull up to 2.5V on baseboard
A56	RESERVED_A56	VIN_SENSE	OCVR input Analog sense
B57	RESERVED_B57	L2_SENSE	VCC_L2 remote sense
B83	RESERVED_B83	CORE_AN_VSENSE	OCVR output remote sense
B164	EMI	RESERVED_B164	Do not connect
B165	EMI	RESERVED_B165	Do not connect

1. Information in table is for reference only. Refer to the appropriate processor datasheet for valid specifications.

Table 9: New Pin Definition Considerations

System Design	Implications
• Pentium® III Xeon™ processor with 256KB L2 cache systems with Pentium III Xeon processor at 500 MHz and 550 MHz support. • Pentium III Xeon processor with 1MB and 2MB L2 cache systems with Pentium III Xeon processor at 500 MHz and 550 MHz support	For the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache, verify compatible connection for the OCVR_EN, OCVR_OK, VIN_SENSE, L2_SENSE, CORE_AN_SENSE, and SELFSB[1:0] signals (more detail of signal usage is described in Sections 10.1, 11, and 14. Pins formerly labeled as EMI have no effect on the Pentium III Xeon processor with 256KB L2 cache and the Pentium III Xeon processor with 1MB and 2MB L2 cache and can be left unconnected or tied to GND. Verify that pins previously specified as TEST_VCC_CORE_A23 and TEST_VCC_CORE_B27 don't see a voltage higher than 2.8 V. These pins can be tied to either VCC_2.5 (recommended) or VCC_CORE.
• Pentium III Xeon processor with 256KB L2 cache systems without Pentium III Xeon processor at 500 MHz and 550 MHz support • Pentium III Xeon processor with 1MB and 2MB L2 cache systems without Pentium III Xeon processor at 500 MHz and 550 MHz support	Suggested OCVR_EN, OCVR_OK usage is given in section 10.1. TEST_2.5_XX pins should be connected to VCC_2.5V supply through separate 10 Kohm resistors (do not connect to VCC_CORE).

9.0 TEST_VCC Pins A23 and B27

Intel recommends tying the formerly defined pins TEST_VCC_CORE_A23 and TEST_VCC_CORE_B27 to the VCC_2.5V supply through separate 10 Kohm resistors on the baseboard. For the Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache, these pins are specified as TEST_2.5_XX pins. However, there will be no damage to these processors if platforms based on the Pentium II Xeon pro-

cessor or Pentium III Xeon processor at 500 MHz and 550 MHz provide 2.8V to the pull-up resistors. On systems where VCC_CORE is 5V or 12V, it is strongly recommended to connect TEST_2.5_XX pins to 2.5 V through separate 10 Kohm resistors to prevent potential damage to the processor.

Table 10: TEST_2.5_XX Pins Considerations

System Design	Implications
2.8V Pentium® III Xeon™ processor systems	Systems with these signals tied to VCC_CORE (2.8 V or less) do not require any modifications. Tying these pins to 2.5 V through separate 10 Kohm resistors is recommended.
5/12V Pentium III Xeon processor systems	Connect TEST_2.5_XX pins to 2.5V (not VCC_CORE) through separate 10 Kohm resistors to prevent potential damage to the processor.

10.0 OCVR (On Cartridge Voltage Regulator)

The On Cartridge Voltage Regulator (OCVR) is a new device located inside the Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache cartridge that provides the necessary power delivery precision for the processor core and integrated L2 cache. On both the 2.8V and 5/12V Pentium III Xeon processors, the OCVR regulates VCC_CORE (2.8V or 5/12V) to the required processor core voltage. The previously defined SC330 VCC_CORE pins are used to provide the input voltage to the OCVR.

In order to accommodate legacy support and guarantee stable operation, the OCVR incorporates the control signals discussed below. Refer to Figure 1 and Figure 2 for an illustration of OCVR interaction with legacy and new systems.

10.1 OCVR Control Signals

The control signals are newly defined in the SC330.1 specification. They provide reliable operation of the OCVR and cartridge connectivity in existing and new platforms.

10.2 OCVR_OK (Pin B3)

This is a valid high signal pulled up on the cartridge to VCC_SMB. The OCVR is not expected to provide a valid OCVR_OK signal assertion within 13 ms of seeing 90% of its input voltage. The OCVR_OK signal is also not guaranteed to be valid until 0.5 ms (max) after Vin to the OCVR reaches 90% of its nominal voltage. Prior to this time, it is possible for the OCVR_OK signal to be incorrectly asserted (high). This signal is also logically AND-gated with the PWRGOOD input signal to guarantee a valid PWRGOOD assertion when the cartridge is installed in existing platforms. The OCVR output must be valid and stable before the processor will receive an asserted

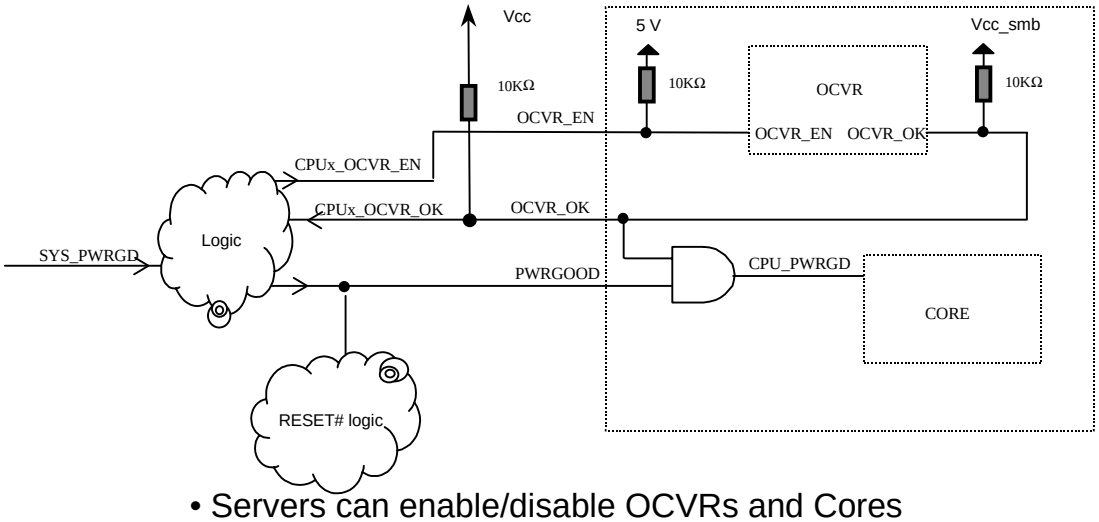
PWRGOOD signal. However, the baseboard needs to make sure there is enough delay between the valid PWRGOOD seen at the core and the release of the RESET# signal from the baseboard. (Refer to Figure 3 and Section 10.4 for further details). In new platforms, the OCVR_OK signal should be used in any power logic that determines the assertion of PWRGOOD to avoid power sequencing concerns and determine proper generation of RESET#.

10.3 OCVR_EN (Pin A26)

The OCVR_EN signal provides a means to disable the OCVR in new systems. This is a valid high signal pulled up to 5V through a 10 Kohm resistor on the cartridge. The OCVR_EN signal provides a safe mechanism to avoid false OCVR turn-on in new systems where the VRM has been removed from the design. In existing systems, this signal is routed to a previously reserved pin (NC) and the internal pull-up will, by default, enable the OCVR.

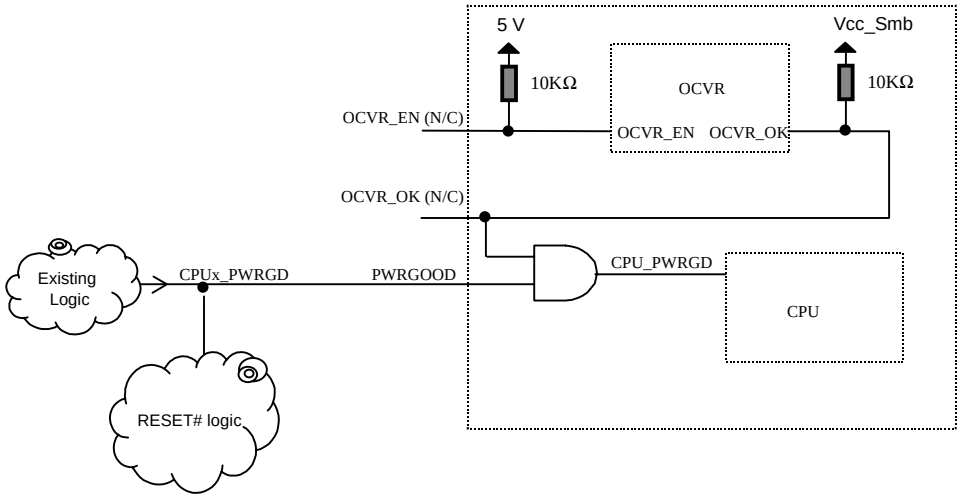
10.4 Power sequencing considerations

The VRM 8.3 specification requires VRM POWERGOOD to go active when its output is within 12% of nominal value. In the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache, PWRGOOD is logically AND-gated with OCVR_OK before being applied to the core's PWRGOOD input. According to legacy datasheet documents, RESET# release must happen a minimum of 1 mS after the core sees PWRGOOD asserted. However, the OCVR is expected to provide a valid OCVR_OK signal a maximum of 13 mS after seeing 90% of its input voltage. This 13 ms max delay OCVR_OK assertion may cause a race condition between RESET# and the asserted POWERGOOD that is seen at the core. For example, systems that do not monitor the OCVR_OK signal and/or account for this additional delay in the PWRGOOD path may end up asserting RESET# prior to 1 ms after PWRGOOD assertion. Therefore, systems should incorporate the OCVR_OK signal in the PWRGOOD/ RESET# generation logic. Those systems that can not incorporate this signals should relax (further delay) the deassertion of processor RESET# to meet this critical constrain. Careful analysis needs to be done in existing platforms. Refer to Figure 3 for the new timing relationship requirements of Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache.



• Servers can enable/disable OCVRs and Cores independently

Figure 1. OCVR Control Lines Implementation (New Systems)



• AND gate implemented to meet legacy system requirements
•protects against early CPU_PWRGD assertion due to PWRGOOD leading OCVR_OK
•allows for independent disable of individual Core through deassertion of PWRGOOD
• Potential for Race condition between CPU_PWRGD and RESET# system dependent. In legacy Systems RESET# timing needs to be reevaluated.

Figure 2. OCVR Control Lines Implementation (Legacy Systems)

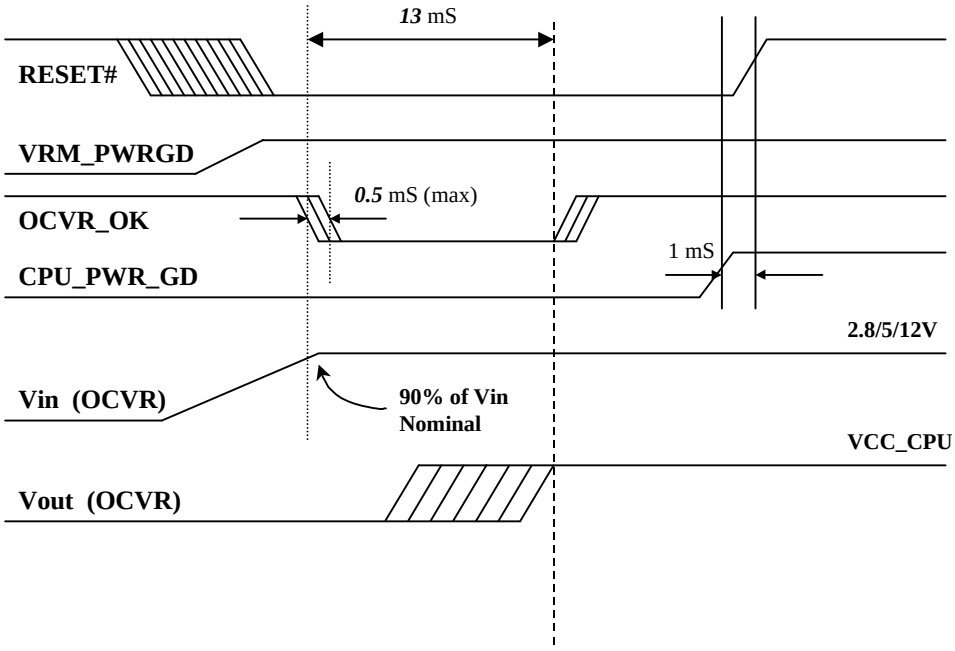


Figure 3. OCVR_OK & POWERGOOD Timing Requirements

Table 11: OCVR Timing Requirements Relative to Baseboard PWRGOOD

System Design	Implications
Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache systems	The valid turn-on time of the OCVR_OK line may cause a race condition between RESET# and the valid PWRGOOD that is seen at the core. It is recommended to relax the deassertion of RESET# to meet this critical constraint. Careful analysis needs to be done in existing platforms. Refer to Figure X for timing relationship requirements. New designs should incorporate appropriate logic (described above) for the OCVR_EN and OCVR_OK signals.

11.0 Remote Sense Lines

The Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache cartridges provide remote sensing capabilities at both the input and out-

put of the OCVR. Please note that neither signal is specified for Pentium II Xeon processor and Pentium III Xeon processor at 500 MHz and 550 MHz and should be should be unconnected on legacy platforms.

11.1 VIN_SENSE

This line is provided to accurately compensate for trace losses and guarantee efficient voltage delivery at the OCVR input. Intel continues to recommend sense feedback to the VRM, from either a location on the SC330 connector or through this pin. This pin's functionality is not available in 5/12V Pentium III Xeon processors.

11.2 CORE_AN_VSENSE

This signal is tied to the VCC seen at the core and represents the output of the OCVR. This signal provides the ability to detect events in which an OCVR may behave out of the expected regulation tolerance. The voltage seen at this pin is the actual operating voltage of the core with integrated L2 cache minus I*R drops due to trace routing in the cartridge.

11.3 L2_SENSE

This line is provided for systems that will support Pentium III Xeon processors at 500 MHz and 550 MHz. It allows monitoring the delivery of VCC_L2 voltage on the Pentium III Xeon processor at 500 MHz and 550 MHz. This line is NOT specified in legacy systems and is not recommended connected on Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache systems that will not support Pentium III Xeon processors at 500 MHz and 550 MHz.

Table 12: Remote Sense Lines Considerations

System Design	Implications
• Pentium® III Xeon™ processor with 256KB L2 cache systems without Pentium II Xeon and Pentium III Xeon processor at 500 MHz and 550 MHz • Pentium III Xeon processor with 1MB and 2MB L2 cache systems without Pentium II Xeon and Pentium III Xeon processor at 500 MHz and 550 MHz support	None
• Pentium III Xeon processor with 256KB L2 cache systems with Pentium II Xeon and Pentium III Xeon processor at 500 MHz and 550 MHz support • Pentium III Xeon processor with 1MB and 2MB L2 cache systems with Pentium II Xeon and Pentium III Xeon processor at 500 MHz and 550 MHz support	L2_SENSE can be used as feedback for the L2 VRM on systems supporting Pentium III Xeon at 500 MHz and 550 MHz processors.

12.0 2.5V Signal Voltage Clamps

12.1 Signal Timings and I/O Capacitance

The Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache cartridges contain a new 2.5 V signal voltage clamp device intended to provide 2.5V-signal level compatibility between platforms and the processor core, which uses 1.5 V level signals. The voltage clamp helps reduce overshoot levels seen at the core. These clamps are included on CMOS, TAP, and APIC (PICD[1:0]) signals and result in an increased I/O Capacitance value (Con) compared to previous Pentium II Xeon processors and Pentium III Xeon at 500 MHz and 550 MHz processors. Con is approximately 25 pF max. This max value includes the total capacitance contribution from the voltage clamp and processor core buffer. It does not include cartridge trace capacitance, which is 3 pF/inch and approximately 4 inches total length. This Con value applies to all CMOS, TAP, Clock, and APIC signals except BCLK and PICCLK, which are not connected to the voltage clamp devices.

The Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache PICD[1:0] Valid Delay timing specification is different from the Pentium II Xeon and Pentium III Xeon at 500 MHz and 550 MHz processors. The Pentium III Xeon processor with 1MB and 2MB L2 cache Valid Delay timings differentiate between rising and falling-edge transitions as follows:

PICD[1:0] Valid Delay (Rising Edge) = 8.7 ns

PICD[1:0] Valid Delay (Falling Edge) = 12.0 ns

Please note that these timings are still specified at the core pin with a 150 ohm resistor load pulled-up to 2.5V. In addition, the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache PICD[1:0] Setup Time is much lower at 5.0 ns compared to 8.0 ns for the Pentium II Xeon processor and Pentium III Xeon processor.

Signal specifications contained in this section are for reference only. Refer to the appropriate processor datasheet for valid specifications.

12.2 Design Impact

The additional I/O capacitance associated with the voltage clamp will increase the signal propagation time (compared to a Pentium III Xeon processor at 500 MHz and 550 MHz system) since the RC time constant of the signal path increases. This increased capacitance will most likely impact the APIC bus since it is synchronous and uses PICCLK. The increased propagation time may affect receiver setup margin. APIC bus flight time will likely be limited by rising edge transitions since the resistance term used would be the effective pull-up resistance on this signal (assumed to be 150 ohms). The resistance term for falling edges is equal to the core nMOS on-resistance plus voltage clamp on-resistance (approximately 25 ohms).

Improvements to the rising edge PICD Valid Delay spec will provide some relief to the RC propagation delay effects. Also, the improved PICD setup time will provide substantial relief to timing paths where the processor is the receiving agent. However, since APIC behavior is strongly dependent on baseboard layout and APIC components chosen, Intel highly recommends that system designers perform an analysis to better understand the impact of these changes. The following section provides two examples for performing a first-pass timing calculation.

12.3 Design Examples

The following analysis for a 4-way Pentium III Xeon processor with 1MB and 2MB L2 cache system will help determine the impact to various systems and APIC bus topologies. A similar analysis can be performed for other system configurations by appropriately entering the required parameters.

For APIC bus timing analysis, the system flight time is broken into two components: straight propagation delay (T_{PROP}), and delay due to the RC time constant of the bus (T_{RC}). See Equation 1 below. T_{RC} is derived from the effective pull-up resistance and the total system capacitance.

Nevertheless, this simple analysis is meant as a starting point for understanding capacitance loading effects and should be reinforced by APIC bus simulations.

Equation 1. Total System Flight Time

$T_{SYSTEM} = T_{PROP} + T_{RC}$

•T_{PROP} = (Longest point-to-point distance) * (Worst-case propagation delay)

•T_{RC} is derived from solving $V(t) = V(0)e^{-T_{RC}/t}$ for T_{RC}.

$\Rightarrow T_{RC} = - t \ln [V(t)/V(0)]$

V(0) = 2.5V since the signal is terminated to 2.5V.

V(t) = 1.25V since this is the voltage reference used for timings.

$t = R_{EFF} * C_{TOTAL}$ and $C_{TOTAL} = C_{T\text{-}LINE} + C_{CPU}$

4-way Example:

Consider a 4-way system with the following APIC bus parameters:

Total trace routing of 30 inches. This defines the total trace length contribution from all individual trace segments (e.g., processors, termination resistor stubs, SC330.1 connectors, and additional APIC agent routing). This total length already includes four Pentium III Xeon processor with 1MB and 2MB L2 cache cartridges, each with 4 inches (720 ps) total trace between the core and edge finger.

• Longest component point-to-point routing distance of 20 inches.

• Nominal board impedance of 60 ohms.

• Worst-case (slowest) propagation delay of 180 ps/inch.

• Transmission line capacitance of 3.0 pF/inch (From the above impedance and propagation delay).

• Effective pull-up resistance of 150 ohms.

For this board design:

T_{PROP} = 20 inches * 180 ps/inch = 3.60 ns

$C_{T\text{-}LINE}$ = 30 inches * 3 pF/inch = 90 pF

C_{CPU} = 4 processors * 25 pF = 100 pF

C_{TOTAL} = 90 pF + 100 pF = 190 pF

t = 150 ohms * 190 pF = 28.5 ns

T_{RC} = 19.8 ns

T_{SYSTEM} = 3.60 ns + 19.8 ns = 23.4 ns

Using the simple timing equation below (with driver T_{CO}, T_{SYSTEM}, and receiver T_{SETUP}), this system shows margin running at 25.0 MHz (40.0 ns period). This timing equation specifically applies to the processor-to-processor flight path. Timing analysis involving additional APIC agents requires using their appropriate timing parameters in the timing equation below. Note that clock skew and jitter effects must still be considered.

$T_{CO} + T_{SYSTEM} + T_{SETUP} = T_{PERIOD}$

8.7 ns + 23.4 ns + 5.0 ns = 37.1 ns

Margin to 25.0 MHz = 40 ns - 37.1 ns = 2.9 ns

Table 13: Voltage Clamp Considerations

System Design	Implications
Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache systems.	Since the voltage clamp introduces additional delay (loading) on 2.5 V signals, Intel recommends complete validation, testing and signal integrity analysis to ensure that the specifications published in the processor datasheets are fully met. Since APIC bus signals are synchronous, verify layout will meet Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache setup and hold timings.

13.0 2.5V Signal Output Low Voltage

The CMOS, TAP, and APIC signal VOL (Output Low Voltage) capability of the Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache is weaker than the previous Pentium III Xeon processor at 500 MHz and 550 MHz specification. The *Pentium III Xeon Processor at 500 MHz and 550 MHz Datasheet* specifies a V_{OL} of 0.5V while sinking 24 mA. The V_{OL} specification for the Pentium III Xeon processor with 1MB and 2MB L2 cache is 0.55V while sinking 20 mA for the APIC PICD signals, and 0.5V while sinking 14 mA for the CMOS and TAP signals. Another change is that V_{OL} specifications are now defined at the processor edge fingers for the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache in order to comprehend the electrical effects of the voltage clamp device.

Table 14: 2.5V Signal VOL

System Design	Implications
Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache systems	Since the V_{OL} capability for the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache is less than the Pentium III Xeon processor at 500 MHz and 550 MHz, make sure the baseboard layout, timing, and termination for the CMOS, TAP, and APIC buses will satisfy the V_{ILMAX} requirements for all devices interfacing with these signals. A bus designed to the Pentium III Xeon processor at 500 MHz and 550 MHz V_{OL} specification may not support the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache if the pull-up resistance is too strong (i.e., if the resistance value is small). Since 2.5V signal bus design is dependent on the electrical requirements of the devices which interface with the processor, perform a DC (e.g., paper calculation) and AC (simulation and measurements) signal analysis to identify any potential problems.

14.0 SELFSB[1:0] Pins Implementation

14.1 SELFSB[1:0] Functionality

The new definition of the SELFSB [1:0] pins is compatible with legacy systems as well as new platforms. This definition provides the means for the clock synthesizer and additional baseboard logic to auto detect the expected system bus frequency required by a specific cartridge. In addition, this implementation eliminates a baseboard jumper that would be necessary to select between a Pentium III Xeon processor that only supports 100 MHz system bus frequency versus a Pentium III Xeon processor that only supports 133 MHz.

As an output from the cartridge, the value of SELFSB1 offers a way for baseboards to automatically determine the correct system bus frequency (100 MHz or 133 MHz). The SELFSB1 signal is grounded on processors that support 100 MHz system bus frequency, no-connect on processors that support 133 MHz. See Table 15 for processor SELFSB1 details.

The processors use SELFSB0 (input) to select system bus frequency. A high signal applied to this input pin is required to operate the processor at the supported frequency. Table 16 summarizes SELFSB0 functionality.

Table 15: SELFSB1 Functionality Summary

Processor	Pin	Pin Name	Functionality
Pentium® III Xeon™ processor with 256KB L2 cache	A7	SELFSB1	Output: Frequency Identifier N/C (floating) on cartridge (identifies 133 MHz)
Pentium II Xeon and Pentium III Xeon processor at 500 MHz and 550 MHz	A7	SELFSB1 (previously VSS)	Output: Frequency Identifier Grounded on cartridge (identifies 100 MHz)
Pentium III Xeon processor with 1MB and 2MB L2 cache	A7	SELFSB1	Output: Frequency Identifier Grounded on cartridge (identifies 100 MHz)

Table 16: SELFSB0 Functionality Summary

Processor	Pin	Pin Name	Functionality
Pentium® III Xeon™ processor with 256KB L2 cache	A9	SELFSB0	Input: Frequency Selection High: 133 MHz operation Low: 100 MHz operation (unsupported)
Pentium II Xeon processor and Pentium III Xeon processor at 500 MHz and 550 MHz	A9	SELFSB0 (previously Reserved)	Input: Frequency Selection High: 100 MHz operation Low: 66 MHz operation (unsupported)
Pentium III Xeon processor with 1MB and 2MB L2 cache	A9	SELFSB0	Unconnected on processor cartridge (100 MHz operation only)

14.2 SELFSB[1:0] Baseboard Recommendation

The recommended SELFSB[1:0] baseboard implementation is summarized as follows:

SELFSB1: Pull up to 2.5V through 3.3 Kohm resistor. Add resistor dividers as needed to supply the correct high/low voltage values to additional components using this signal (e.g., Intel 840 MCH).

SELFSB0: Pull up to 2.5V through 500 ohm resistor.

Table 17 gives the SELFSB[1:0] line levels when each of the various processors are installed in a new or legacy system. For “New Systems”, the table assumes the baseboard follows the recommendations given in this section.

Table 17: SELFSB[1:0] Signal Values

SELFSB[1:0] levels seen on New Systems		
	SELFSB1(A7)	SELSFB0(A9)
Pentium® III Xeon™ processor with 256KB L2 cache	1	0
Pentium III Xeon processor at 500 MHz and 550 MHz	0	1
Pentium III Xeon processor with 1MB and 2MB L2 cache	0	1
SELFSB[1:0] levels seen on Legacy Systems		
	SELFSB1(A7)	SELSFB0(A9)
Pentium III Xeon processor with 256KB L2 cache	0	Floating (N/C)
Pentium III Xeon processor at 500 MHz and 550 MHz	0	Floating (N/C)
Pentium III Xeon processor with 1MB and 2MB L2 cache	0	Floating (N/C)

The following figures illustrate the recommended SELFSB[1:0] baseboard implementation, along with the results of various processor and baseboard combinations. The Pentium III Xeon processor with 256KB L2 cache is only supported at 133 MHz system bus frequency and may not function at 100 MHz. Also, the Pentium III Xeon processor with 1MB and 2MB L2 cache is only supported

at 100 MHz system bus frequency and may not function at 133 MHz. Note that a “legacy system” refers to a platform originally designed for the Pentium III Xeon processor at 500 MHz and 550 MHz, whereas a “new system” refers to a platform originally designed for the Pentium III Xeon processor with 256KB L2 cache or Pentium III Xeon processor with 1MB and 2MB L2 cache.

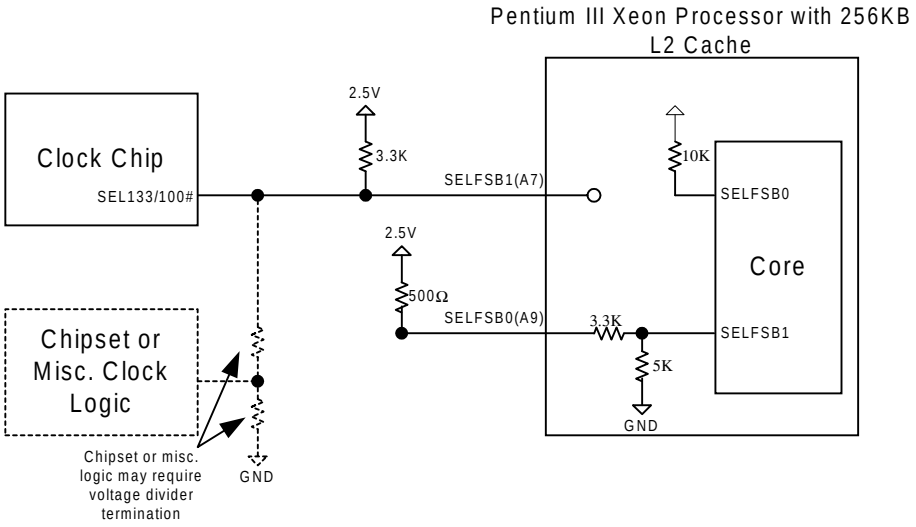


Figure 4. New system with Pentium® III Xeon™ processor with 256KB L2 cache installed (133 MHz selected)

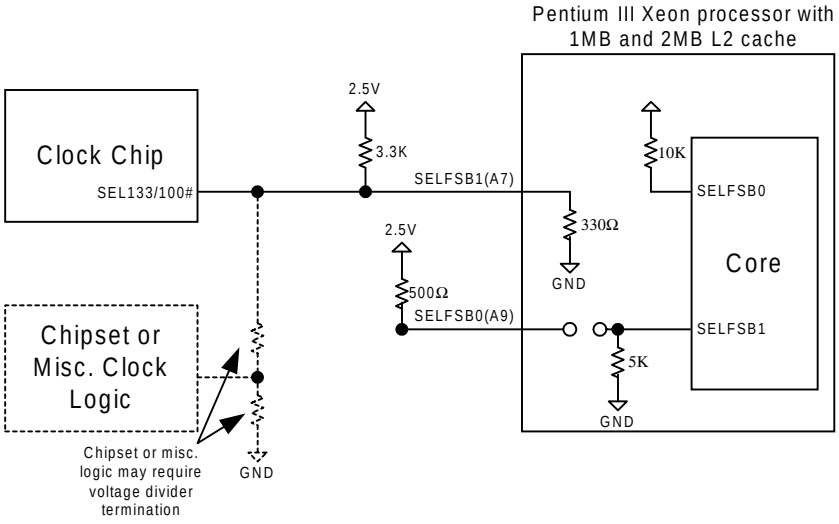


Figure 5. New system with Pentium® III Xeon™ processor with 1MB and 2MB L2 cache installed (100 MHz selected)

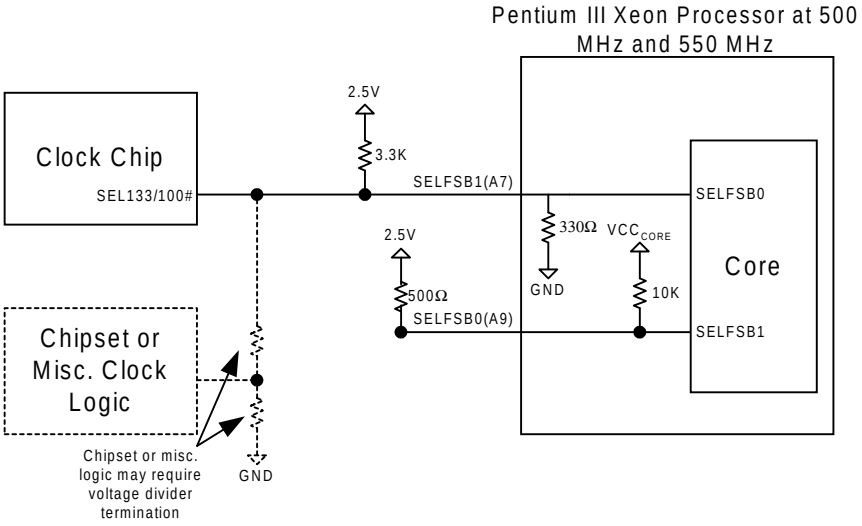


Figure 6. New system with Pentium® III Xeon™ processor at 500 MHz and 550 MHz installed (100 MHz selected)

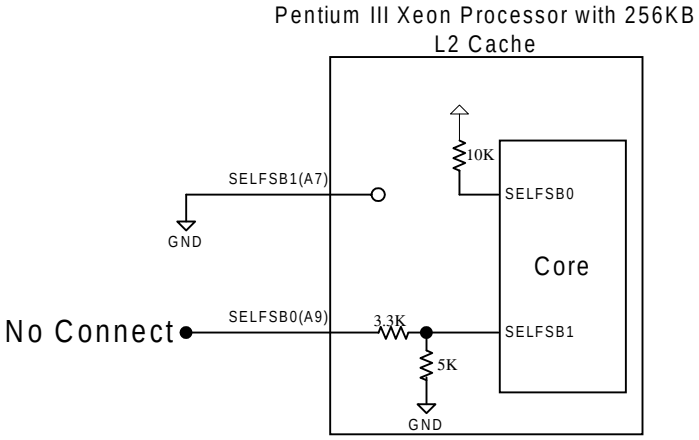


Figure 7. Legacy system with Pentium® III Xeon™ processor with 256 KB L2 cache installed (100 MHz selected)

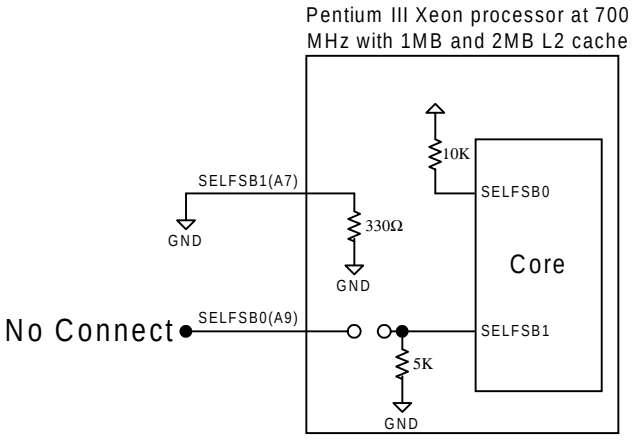


Figure 8. Legacy system with Pentium® III Xeon™ processor with 1MB and 2MB L2 cache installed (100 MHz selected)

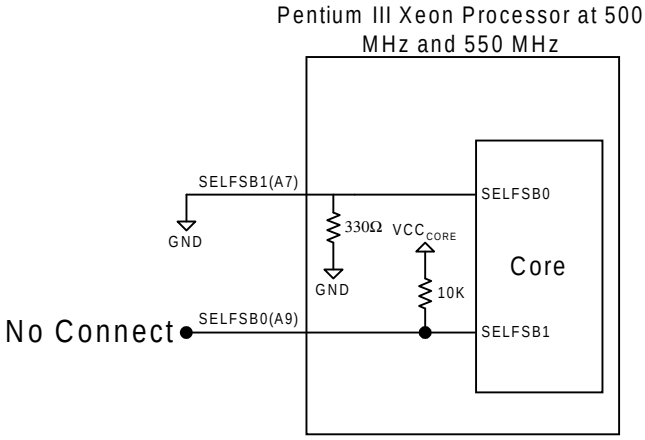


Figure 9. Legacy system with Pentium® III Xeon™ processor at 500 MHz and 550 MHz installed (100 MHz selected)

15.0 SC330 vs. SC330.1 Termination Cards

The previous section discusses the SELFSB[1:0] signals and their intended implementation. For systems that will support the Pentium® III Xeon™ processor with 256KB L2 cache, a new SC330.1 termination card may be necessary. Earlier revisions of the bus terminator design guidelines define pin A7 as VSS (refer to the *Pentium® III Xeon™ Processor Bus Terminator Design Guidelines* for details). In the event these types of termination cards are installed in a system that connects the SELFSB1 output signal together from both connectors, the SELFSB1 line will always be grounded by the termination card, regardless of whether the processor installed in the other connector is 133 MHz or 100 MHz-capable. To support designs that detect the requested clock frequency from both processors before supplying a clock input, the termination card guidelines have been modified to redefine pin A7 as a NC (no-connect). This allows the SELFSB1 line to float high in the case where a Pentium III Xeon processor with 256KB L2 cache is installed.

16.0 BR0# (I/O), BR[3:1]# (I) Lines

The Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache use the same BR#[3:1] and BR0# methodology implemented for previous generations of SC300 processors. Therefore, BREQ connectivity remains the same. However, a reduced set of signals is used in the Pentium III Xeon processor with 256KB L2 cache since this processor supports 2-way configurations only. Attempting to run these processors in a 4-way configuration will result in unsupported and unpredictable behavior. On a Pentium III Xeon processor with 256KB L2 cache cartridge, only BR0#, BR1# and BR3# (Bus Request) pins drive the

BREQ[3:0]# signals on the system. An assertion to BR2# has not effect since is not seen by the processor. The BR[3]# and BR[1:0]# pins are interconnected in a rotating manner to other processor's BR[3]# and BR[1:0]# pins.

The following table from the Pentium III Xeon processor with 1MB and 2MB L2 cache datasheet shows the rotating interconnect baseboard connectivity between the processor and bus signals for 4-way systems. For 2-way systems, only the BREQ0 and BREQ1 signals need to be implemented.

Table 18: BR[3:0]# Rotating Interconnect, 4-way System[1,2]

Bus Signal	Agent 0 Pins	Agent 1 Pins	Agent 2 Pins	Agent 3 Pins
BREQ0#	BR0#	BR3#	BR2#	BR1#
BREQ1#	BR1#	BR0#	BR3#	BR2#
BREQ2#	BR2#	BR1#	BR0#	BR3#
BREQ3#	BR3#	BR2#	BR1#	BR0#

1. Information in table is for reference only. Refer to the appropriate processor datasheet for valid specifications.
2. During power-up configuration, the central agent must assert its BR0# signal. All symmetric agents sample their BR[3:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. This is summarized in the table below for 4-way systems. All agents then configure their BREQ[3:0]# signals to match the appropriate bus signal protocol.

Table 19: Agent ID Configuration[1]

BR0#	BR1#	BR3#	A5#	Agent ID
L	H	H	H	0
H	H	L	H	1
H	H	L	H	2
H	L	H	H	3

1. Information in table is for reference only. Refer to the appropriate processor datasheet for valid specifications.

17.0 Processor Information ROM Information Changes

The Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache implement previously defined fields in the Processor Information ROM (PI-ROM) to allow visibility of core and OCVR voltage requirements. These features are present in SC330 products, but are used in a different way in the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache. These processors implement the On Cartridge Voltage Regulation (OCVR) device. This provides the flexibility to accommodate products with voltage input of 2.8V for one product version and 5V or 12V for a different product version.

The implementation of the PI-ROM in the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache allow software to view the desired voltage outputs of the VRM feeding the OCVR and of the OCVR itself. Software could compare those values to actual VRM/OCVR outputs (using an A/D converter) to determine if the VRMs and OCVRs are operating correctly. The implementation of the PI-ROM gives system designers a means of determining the proper processor core voltage requirements.

The fields defined for the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache coincide as closely as possible with those for the Pentium III Xeon processor at 500 MHz and 550 MHz. The irrelevant “L2 Cache Voltage” field (for Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache) is replaced with a useful “core voltage” field. The Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache (SC330.1) have a pin (A56, “VIN_SENSE”) which allows the baseboard to directly measure the actual OCVR voltage and a pin (B83, “AN_CORE_VSENSE”) which is an analog representation of the voltage input seen at the core. These voltages can be compared with the desired voltage (indicated by the PI-ROM field) to determine if the OCVR input / output voltage is varying from desired levels.

The following table is an excerpt taken from the PI-ROM table listed in the Pentium III Xeon processor with 1MB and 2MB L2 cache datasheet for reference purposes only. For the entire valid PI-ROM specification, refer to the appropriate processor datasheet.

Table 20: PI-ROM Table Excerpt for the Pentium® III Xeon™ Processor with 1MB and 2MB L2 cache[1]

Offset/Section	# of Bits	Function	Notes
PROCESSOR: 0Eh	48	S-spec/QDF Number	Six 8-bit ASCII characters
	2	Sample/Production	00b = Sample only
	6	Reserved	Reserved for future use

Table 20: PI-ROM Table Excerpt for the Pentium® III Xeon™ Processor with 1MB and 2MB L2 cache[1]

Offset/Section	# of Bits	Function	Notes
	8	Checksum	1 byte checksum
CORE: 16h	2	Processor Core Type	From CPUID
	4	Processor Core Family	From CPUID (Family 6
	4	Processor Core Model	From CPUID (Model 8)
	4	Processor Core Stepping	From CPUID
	2	Reserved	
	16	OCVR option 2 Input Voltage ID	Voltage in mV (0=2.8V, 12000=5/12V
	16	OCVR option 2 Input Voltage Tolerance	Edge finger tolerance in mV, +/- (0=2.8V, 600=5/12V)
	8	Reserved	Reserved for future use
	16	Maximum Core Frequency	16-bit binary number (in MHz)
	16	OCVR option 1 Input Voltage ID	Voltage in mV (2800=2.8V, 5000=5/12V)
	16	OCVR option 1 Input Voltage Tolerance	Edge finger tolerance in mV, +/- (85=2.8V, 250=5/12V)
	8	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
L2 CACHE: 25h	32	Reserved	Reserved

Table 20: PI-ROM Table Excerpt for the Pentium® III Xeon™ Processor with 1MB and 2MB L2 cache[1]

Offset/Section	# of Bits	Function	Notes
	16	L2 Cache Size	16-Bit binary number (in Kbytes)
	8	Reserved	
	16	OCVR Output Voltage ID1	Voltage in mV
	8	OCVR Output Voltage Tolerance, High	Core tolerance in mV, +
	8	OCVR Output Voltage Tolerance, Low	Core tolerance in mV, -
	8	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
FEATURES: 74h	32	Processor Core Feature Flags	From CPUID
	24	Cartridge Feature Flags	
	1	OCVR Present	1= Present 0= Not Present
	1	Serial Signature	1= Present 0= Not Present
	1	Electronic signature present	1= Present 0= Not Present
	1	Thermal Sense Device Present	1= Present 0= Not Present
	1	Thermal Reference Byte Present	1= Present 0= Not Present
	1	OEM EEPROM Present	1= Present 0= Not Present
	1	Core VID present	1= Present 0= Not Present
	1	L2 Cache VID present	Always Zero
	4	Number of Devices in TAP Chain	One 4-bit hex digit

Table 20: PI-ROM Table Excerpt for the Pentium® III Xeon™ Processor with 1MB and 2MB L2 cache[1]

Offset/Section	# of Bits	Function	Notes
	4	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
OTHER: 7Eh	16	Reserved	Reserved for future use

1. Information in table is for reference only. Refer to the appropriate processor datasheet for valid power and thermal specifications.

Table 21: New PI-ROM Information for the Pentium® III Xeon™ Processor with 256KB L2 Cache and Pentium III Xeon Processor with 1MB and 2MB L2 Cache.

System Design	Implications
Pentium® III Xeon™ processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache systems	Systems that rely on PI-ROM information to detect voltage requirements need to evaluate the new fields present in the Pentium III Xeon processor with 256KB L2 cache and Pentium III Xeon processor with 1MB and 2MB L2 cache PI-ROM. Ensure software and/or embedded logic on the baseboard can properly detect the various processors supported by the system.