SC242 Termination Card Design Guidelines

November, 1999

Order Number: 245336-001

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1. INTRODUCTION

The Pentium® II and Pentium III microprocessors include termination circuitry for the processor's AGTL+ bus. In a two-processor system each end of the bus must be properly terminated, whether or not both 242-slot edge connector (SC242) locations have processors installed. This document describes design considerations for a termination card to occupy the second SC242 connector location and terminate the bus when there is only one processor installed in a two-processor system.

Designs should adhere to the bus guidelines in Section 3. However, there are ways to implement a bus termination card other than as shown in this document. The resistor and decoupling network schematics in this document are examples only, and other resistor and decoupling designs are feasible. This document does not provide detail on variations to the specific design solution presented.

This version of the design guidelines includes three changes from the prior version (Intel Order Number 243409-002):

– Pin A14 is open (RESERVED)
– Pin B76 is open (RESERVED)
– Marking instructions ("SC242.1") identify this version.

A termination card consistent with this version supports 66, 100, and 133 Megahertz systems bus frequencies. The BSEL[1:0] description in the datasheet *Pentium III Processor for the SC242 at 350 MHz to 733 MHz*, Table 41 shows processor bus selection details.

2. TERMINATION CARD REFERENCE SCHEMATICS

Figures 1 and 2 show the names of the corresponding signals that interface through the SC242 connector.

Figures 3 and 4 are examples of termination resistor networks implemented with four-resistor packages that have two separate connections for each resistor element. Note that the maximum power for each resistor is 0.05 W (i.e., 0.20 W/four-pack of resistors) and that this is the maximum power per resistor that will need to be dissipated.

Figure 5 is a capacitor decoupling network between V_{TT} and ground to prevent V_{TT} noise interference (voltage drop) on the bus signals. This interference is caused by the potentially large current draw through the V_{TT} power distribution plane (or trace) to the termination resistors.

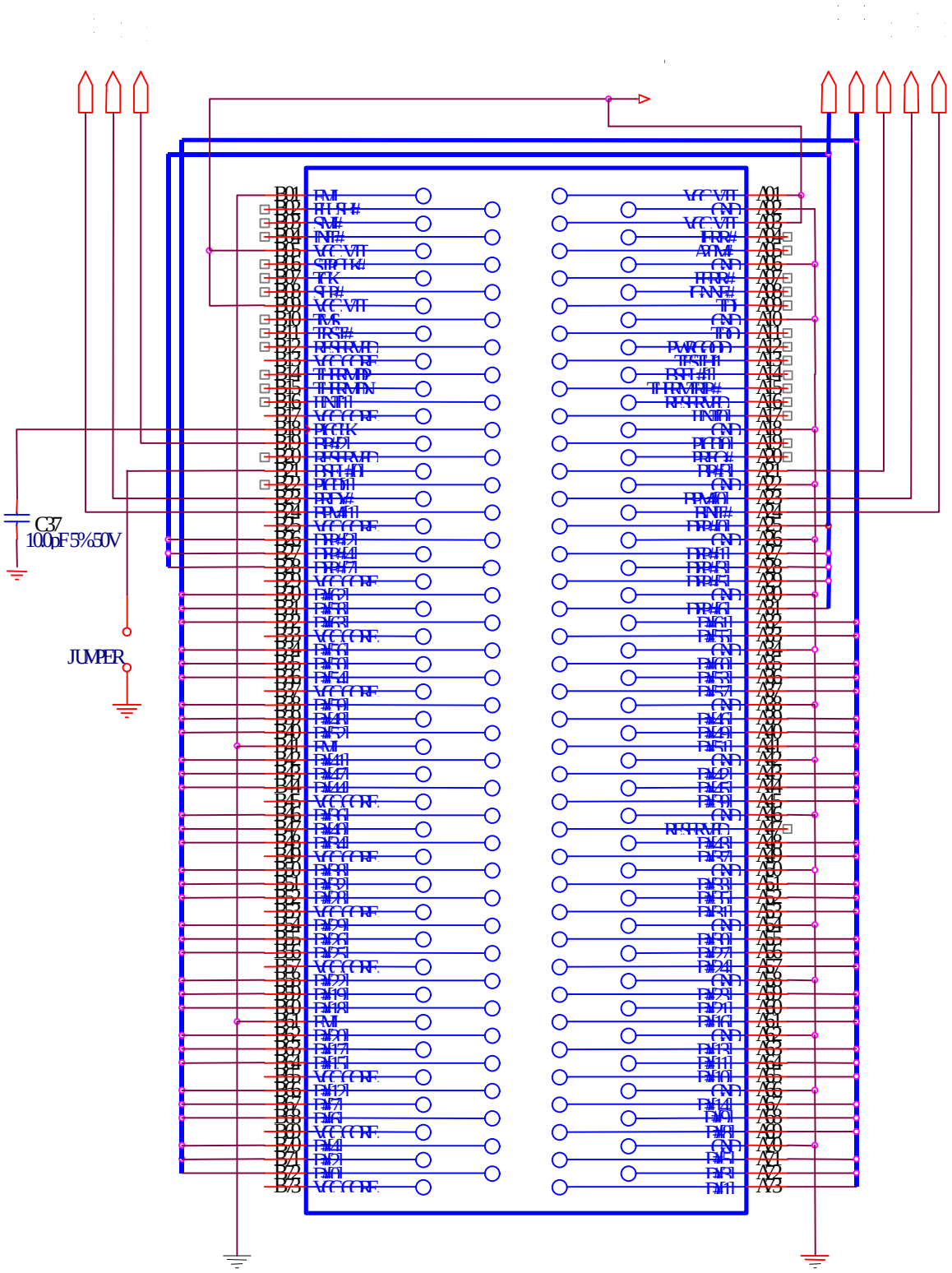

Figure 1, Signals on SC242 Connector (A1-73, B1-73)

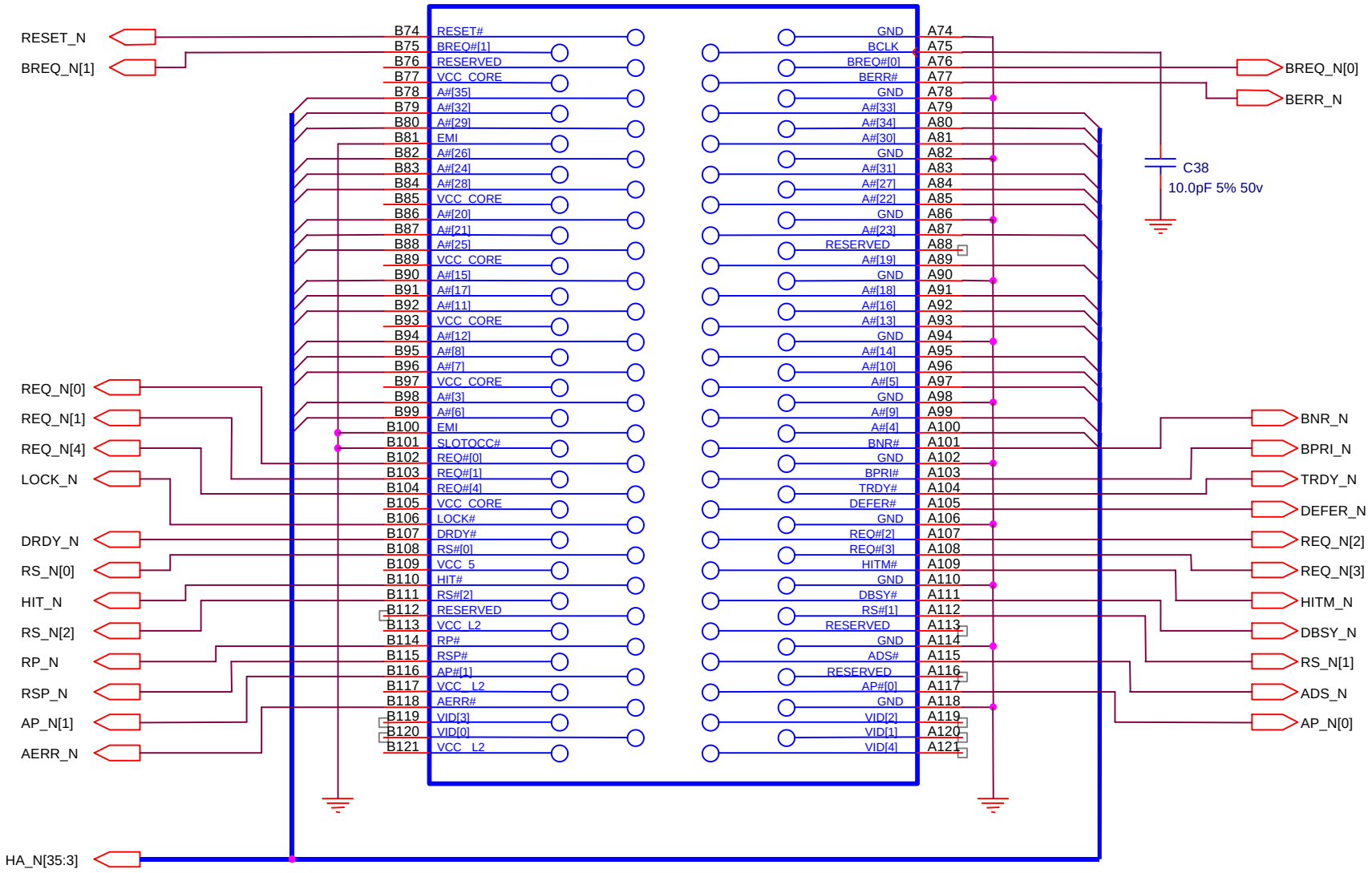

Figure 2, Signals on SC242 Connector (A74-121, B74-121)

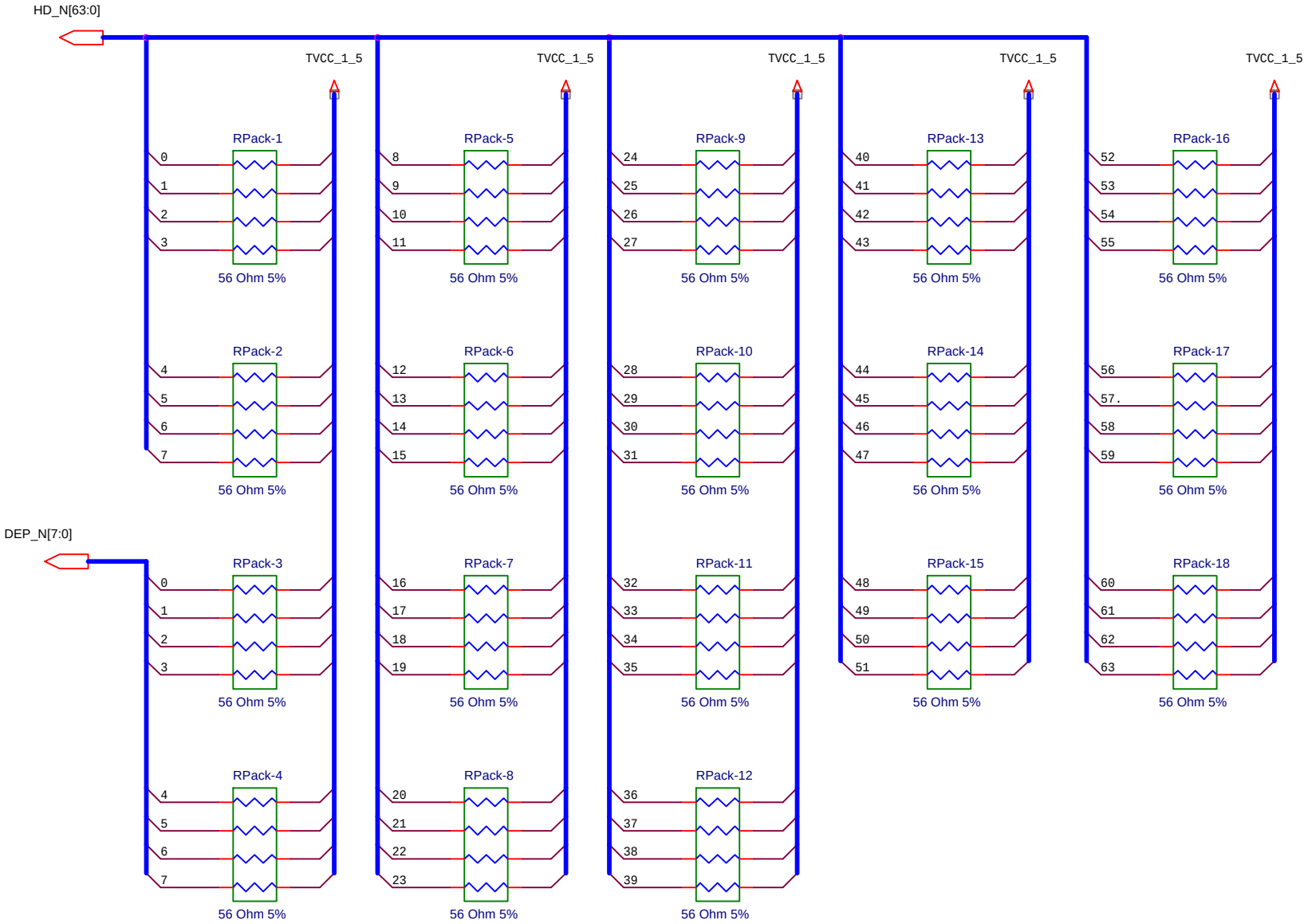

Figure 3, Termination Resistors

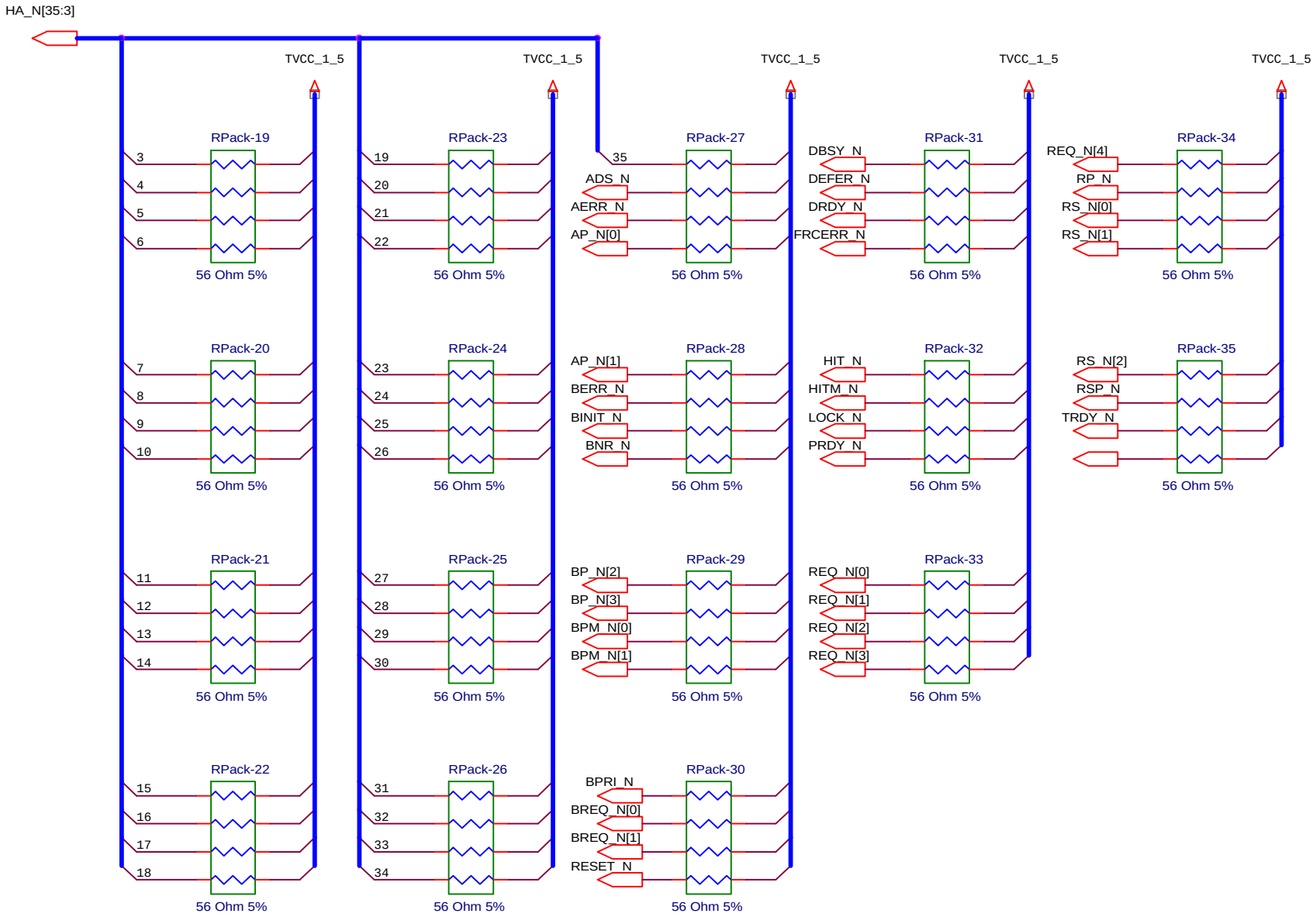

Figure 4, Termination Resistors

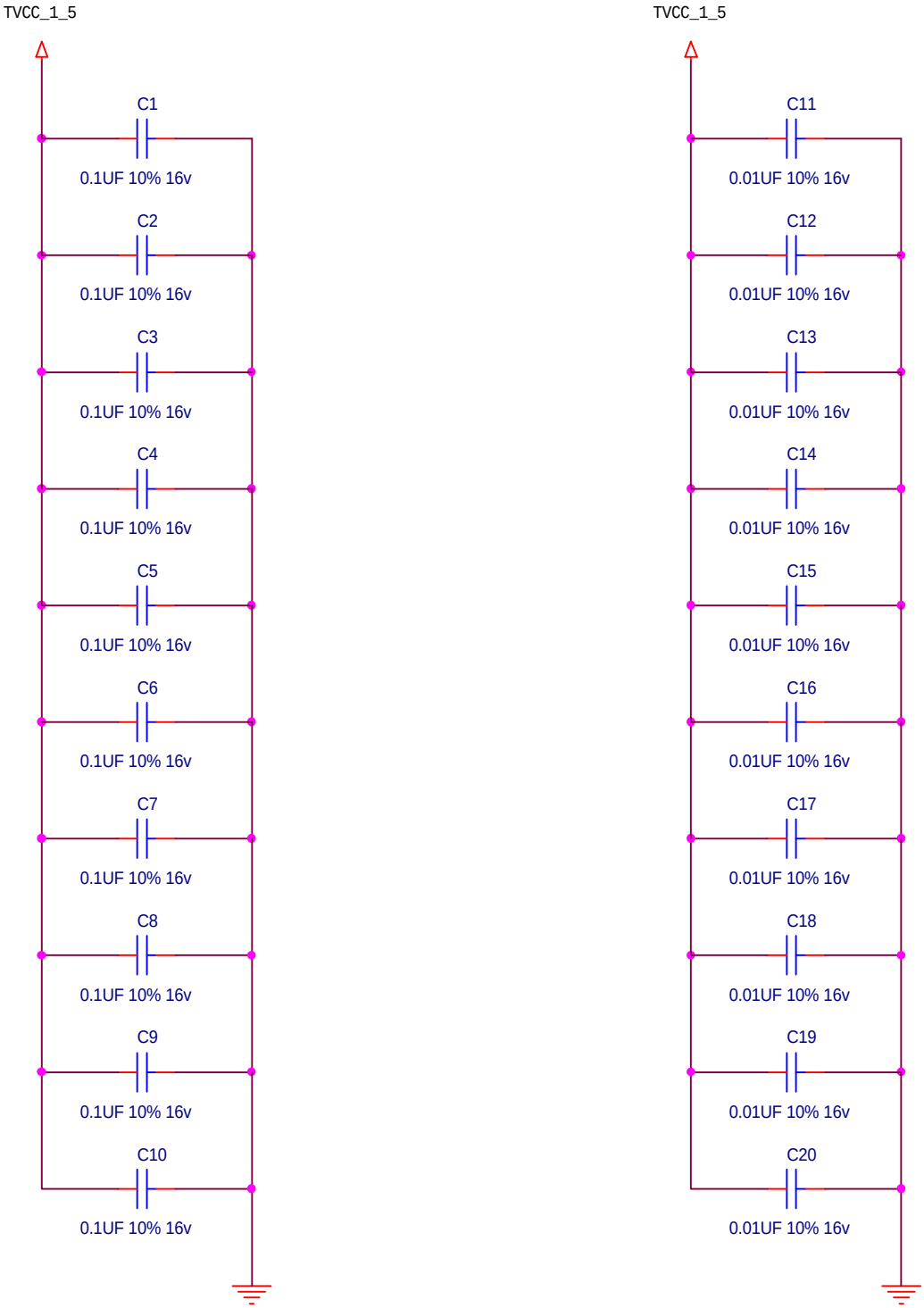

Figure 5, Termination Decoupling

3. AGTL+ BUS GUIDELINES

The design should follow AGTL+ layout guidelines. Some of these guidelines include:

- Limit trace routing length on the card to 1.5 inches.
- Distribute V_{TT} with a wide trace or plane. A plane is recommended; however, a 50 mil minimum width trace may also be used.
- Closely control the characteristic line impedance, Z_0, to a 50Ω - 80Ω range. A ground plane will be needed to maintain the proper characteristic line impedance.
- Make sure power routings are decoupled correctly.
- A PCB signal velocity of 1.6 to 2.2 ns/ft should be used.
- Minimize cross talk:
    1. Maximize line-to-line spacing (at least 10 mils between traces).
    2. Keep the dielectric constant used on the termination card between 4.2 and 4.8.
    3. Minimize the cross sectional area of the traces, (5 mil lines with 1/2 ounce/ft^2 copper – but beware of higher resistively traces).
    4. Eliminate parallel traces between layers if not separated by a power or ground plane.
    5. Isolate AGTL+ signals in groups. That is, route the data signals in one group, the control signals in one group, and the address signals in another group. If the groups are routed together on a plane, provide at least 25 mils separation between the groups.

Please refer to the *Pentium® II Processor AGTL+ Guidelines*, for more information.

Conventional “pull-up” resistor networks may not be suitable for termination. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). The packages generally have too much inductance to maintain the voltage and current needed at each resistive load. Systems usually get better results with discrete resistors, resistor packages with two separate pins for each resistor, or other resistor networks with acceptable characteristics.

4. Termination Card Physical Description

Figure 6 illustrates a physical format template for the termination card. The card edge must mate properly with the 242-pin slot connector (see *SC242 Connector Design Guidelines*). For details on single edge contact cartridge (S.E.C.C.) or S.E.C.C. 2 dimensions please refer to the Pentium® II or Pentium III processor datasheet, respectively.

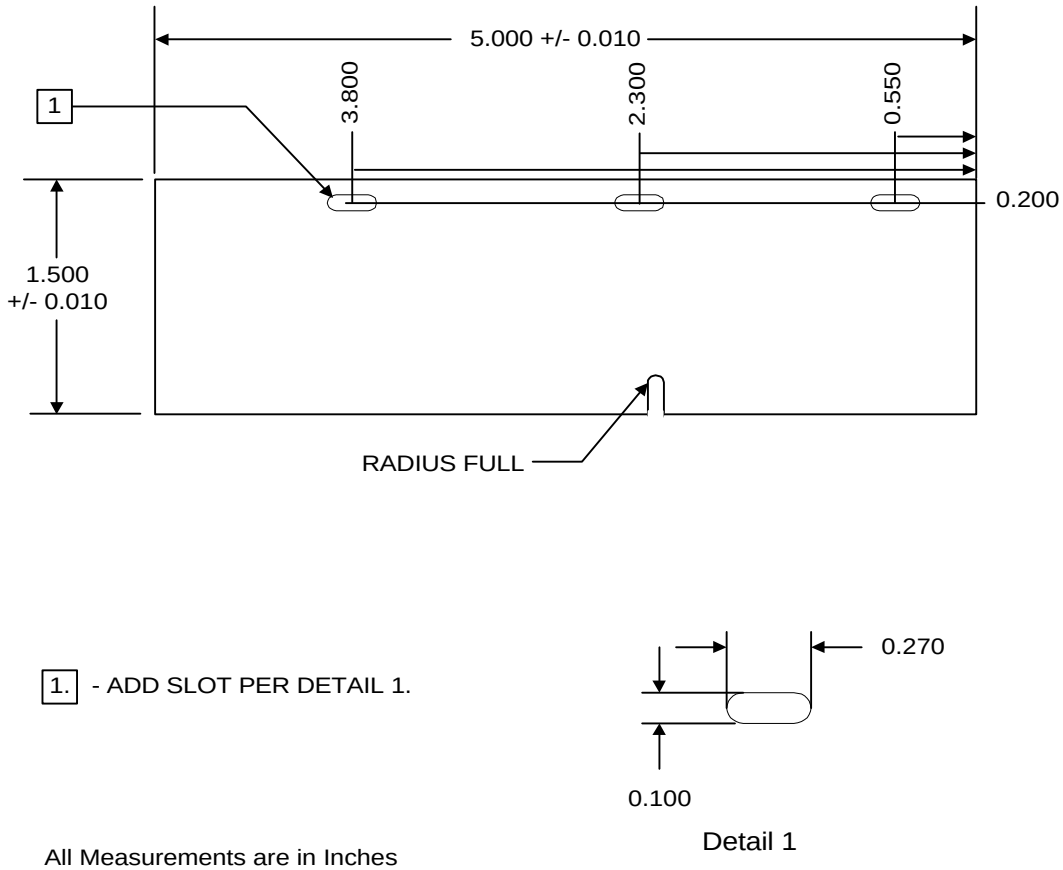

Figure 6, Termination Card Dimensions

5. TERMINATION CARD RETENTION

Computer board and system manufacturers install retention mechanisms on motherboards to ensure the mechanical integrity of systems with S.E.C.C. and S.E.C.C. 2 cartridges. Depending on shock and vibration specifications, the bus termination card might need to latch to the retention mechanism to remain secure. Mechanical shock and vibration specifications are determined by each computer OEM.

The bus termination card should be physically compatible with the same retention mechanism used for the cartridges. For detailed dimensions of retention mechanism reference designs please refer to AP-903, *Mechanical Assembly and Customer Manufacturing Technology For S.E.C.C.2 Package Processors*. For dimensions of actual retention mechanisms, request the appropriate drawings from the suppliers.

6. Reference Documents

Referenced documentation is available from:

http://developer.intel.com/design/PentiumII

or

http://developer.intel.com/design/PentiumIII.

7. Marking

Products complying with this version of the *Design Guidelines* should be conspicuously labeled "SC242.1." Marks may also include the supported bus frequencies: e.g., "66/100/133MHz."

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