

Intel(R) IQ80331 I/O Processor DDR-II 400 Evaluation Platform Board (IQ80331)

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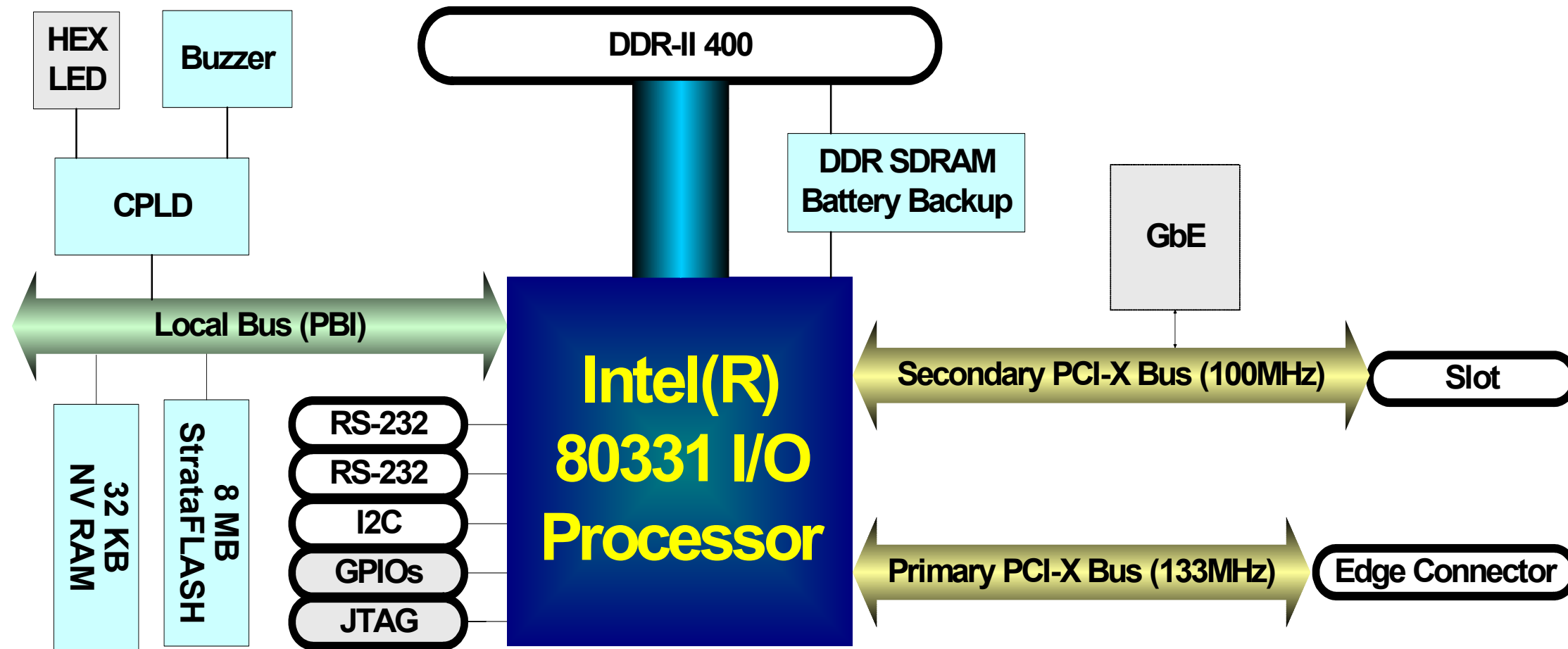
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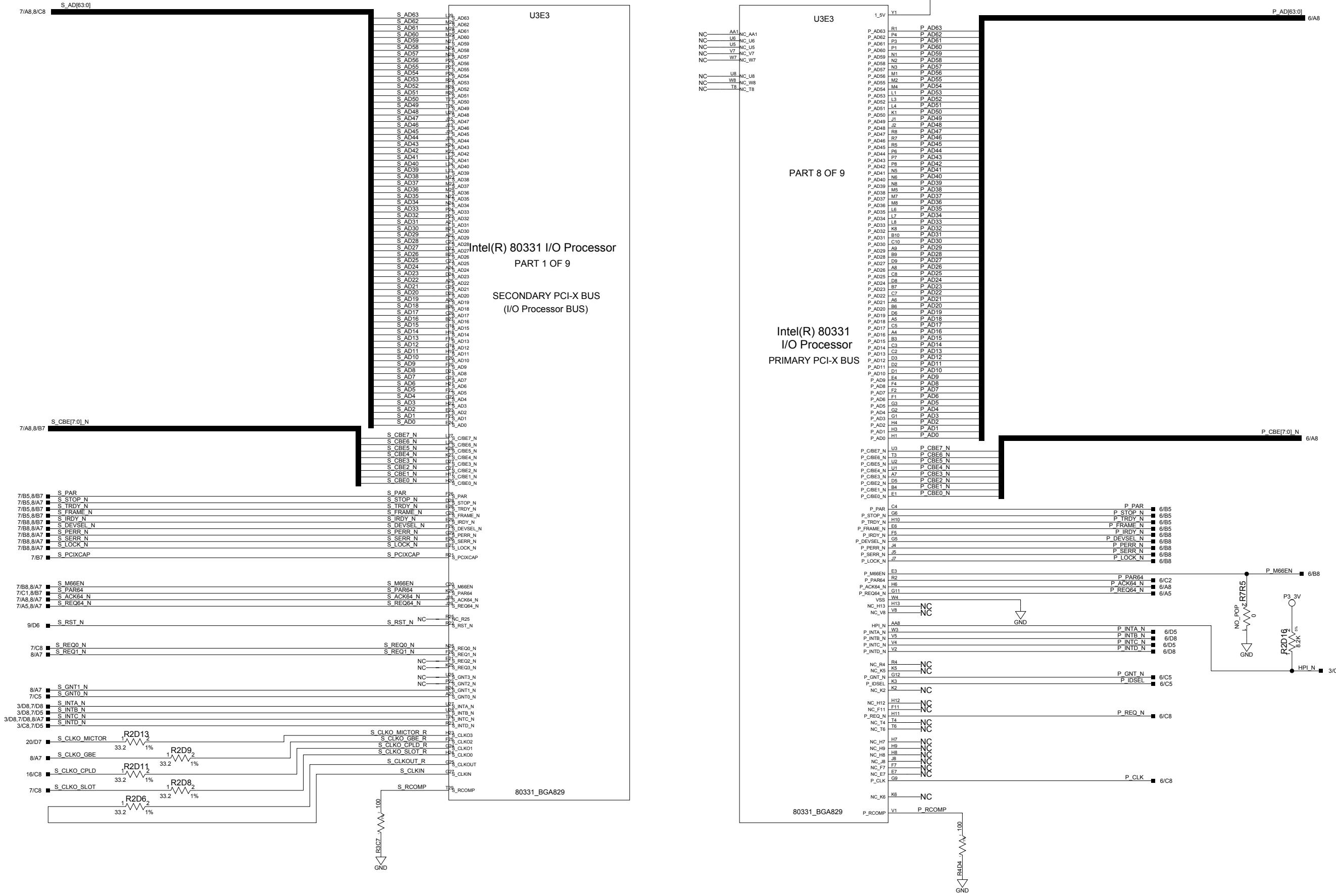
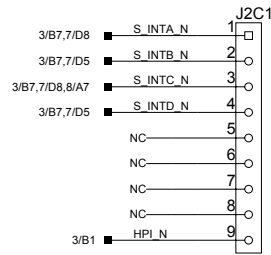
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P1

INTEL(R) IQ80331 DDR-II 400 BLOCK DIAGRAM

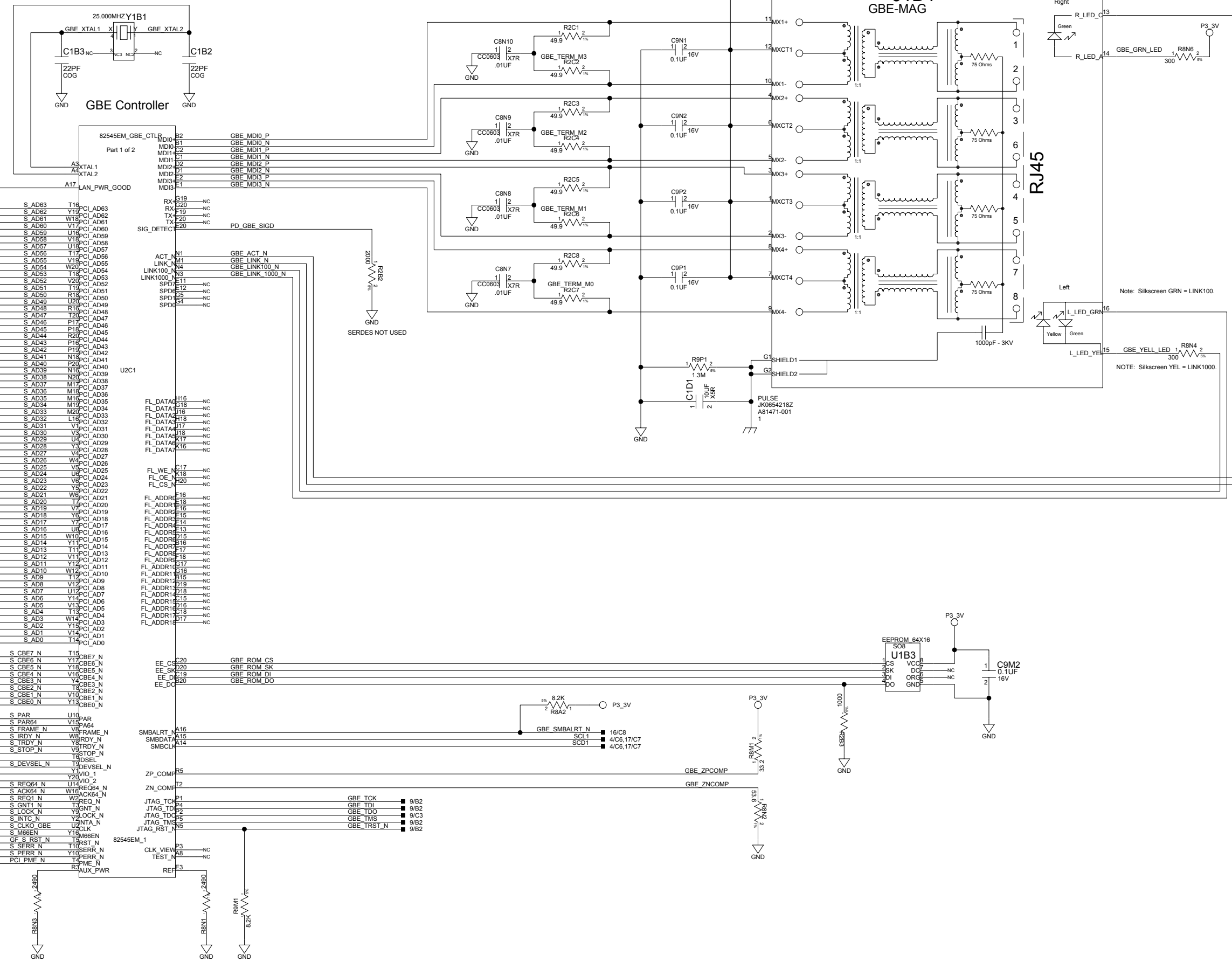


INTERRUPTS HEADER



RJ45 Connector for Gb Ethernet NIC.

NOTE: Isolate this 2.5V plane.

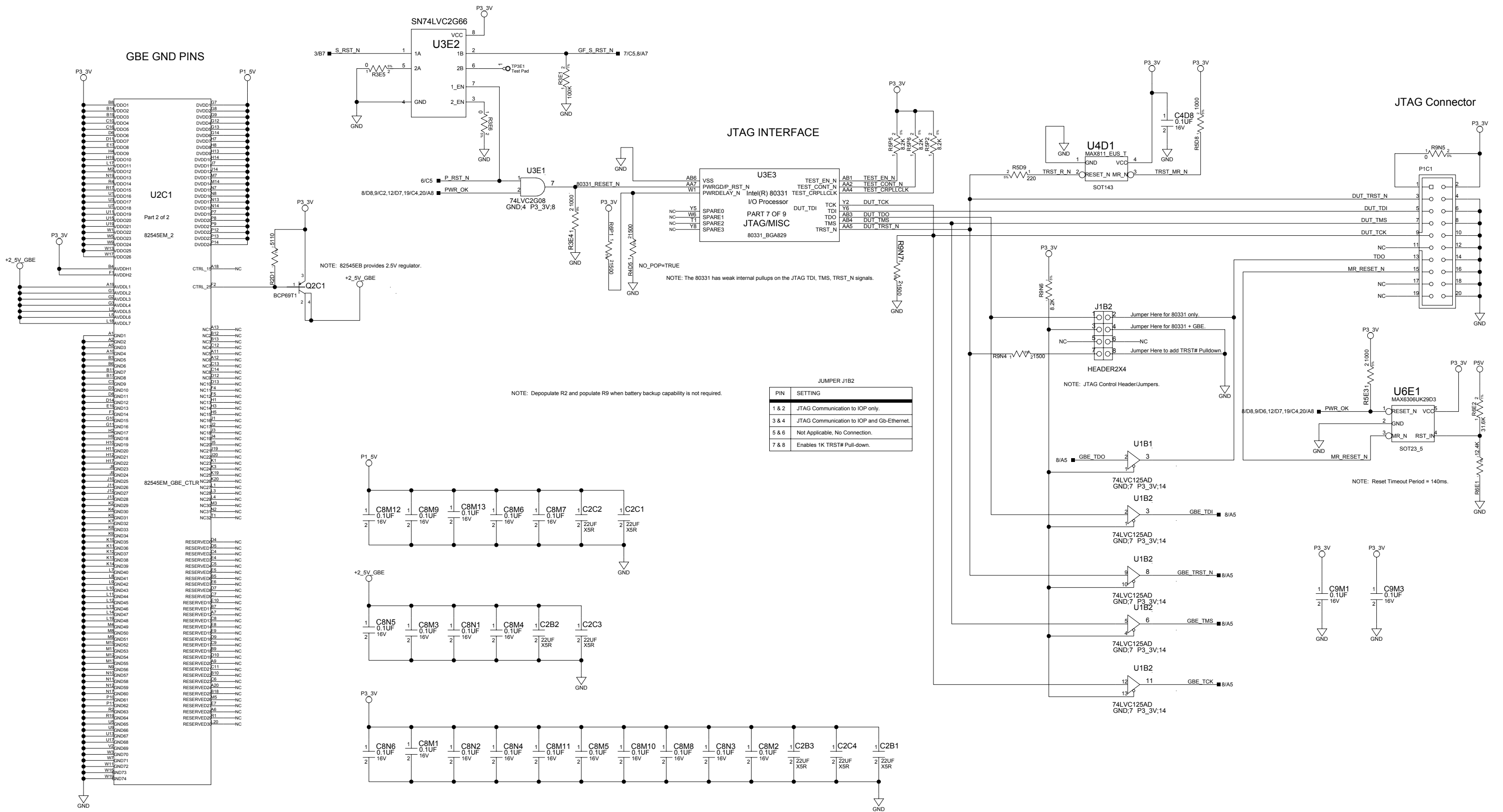


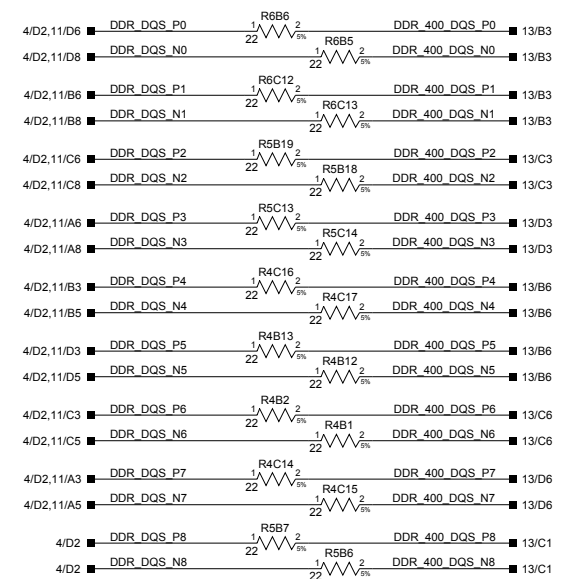
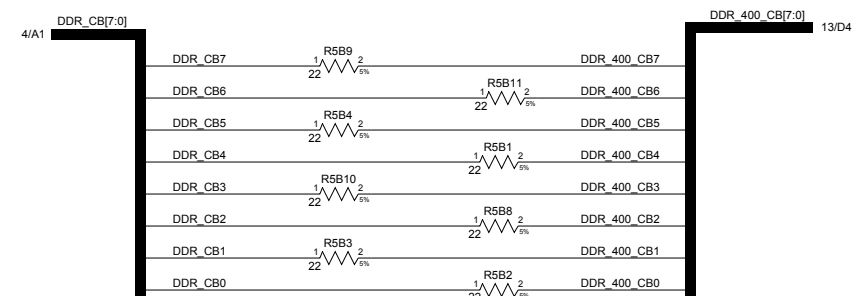
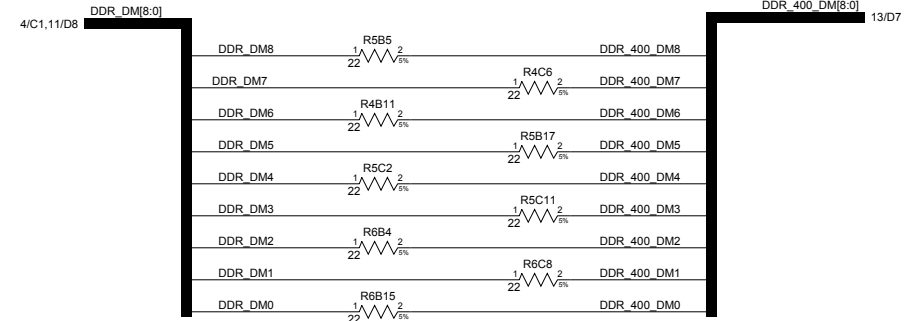
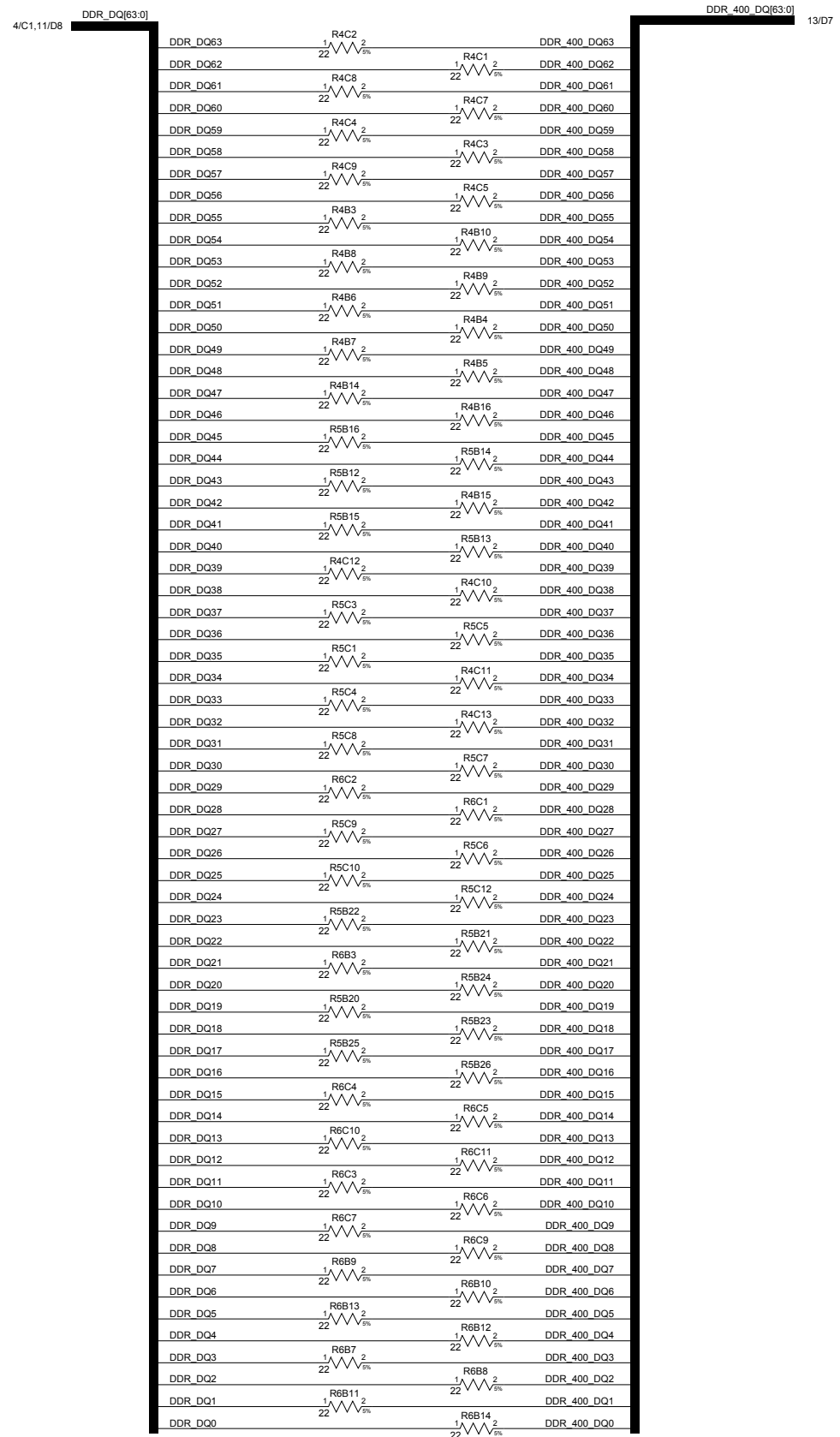
NOTE: Silkscreen as GBE ACT next to LED on device.

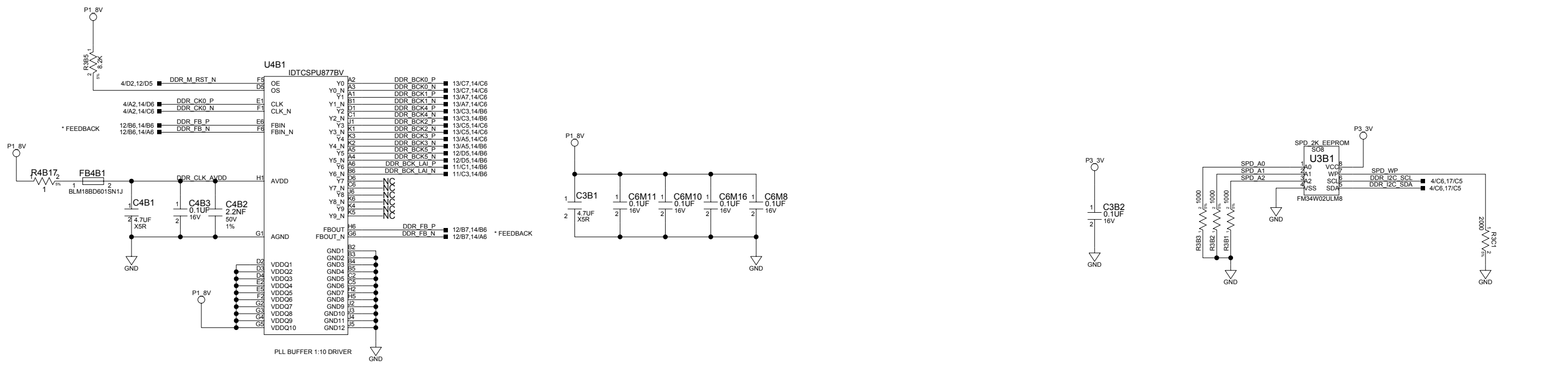
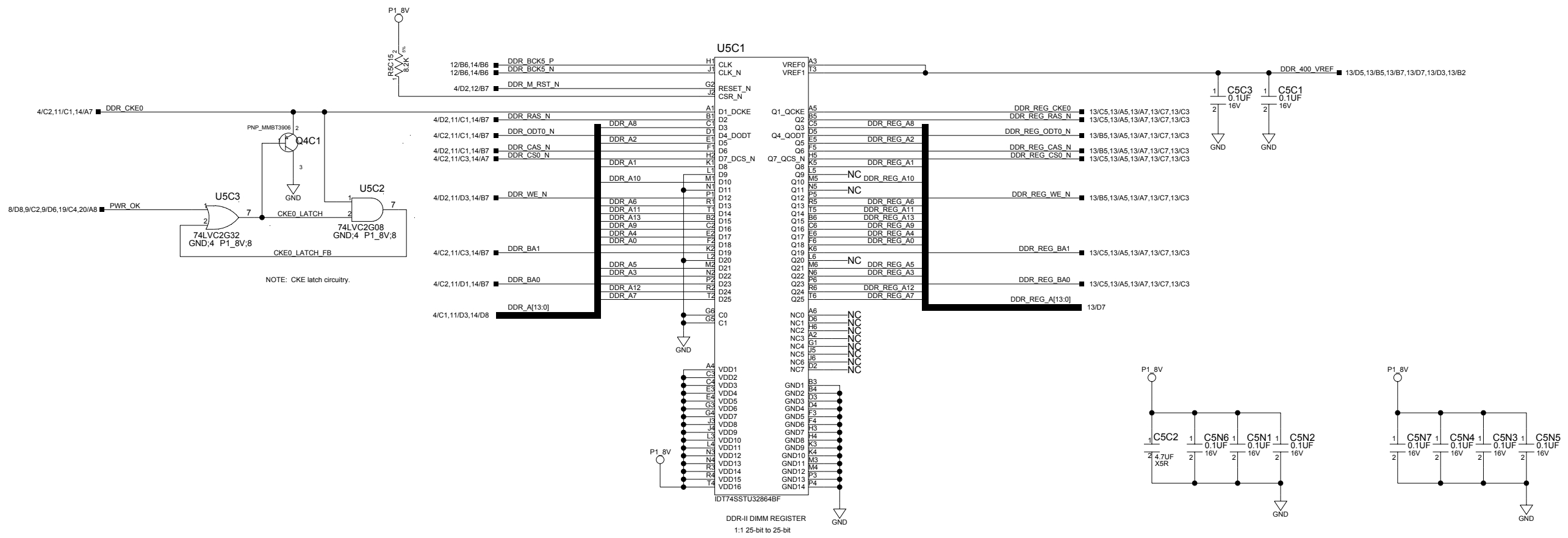
Note: Silkscreen GRN = LINK100.

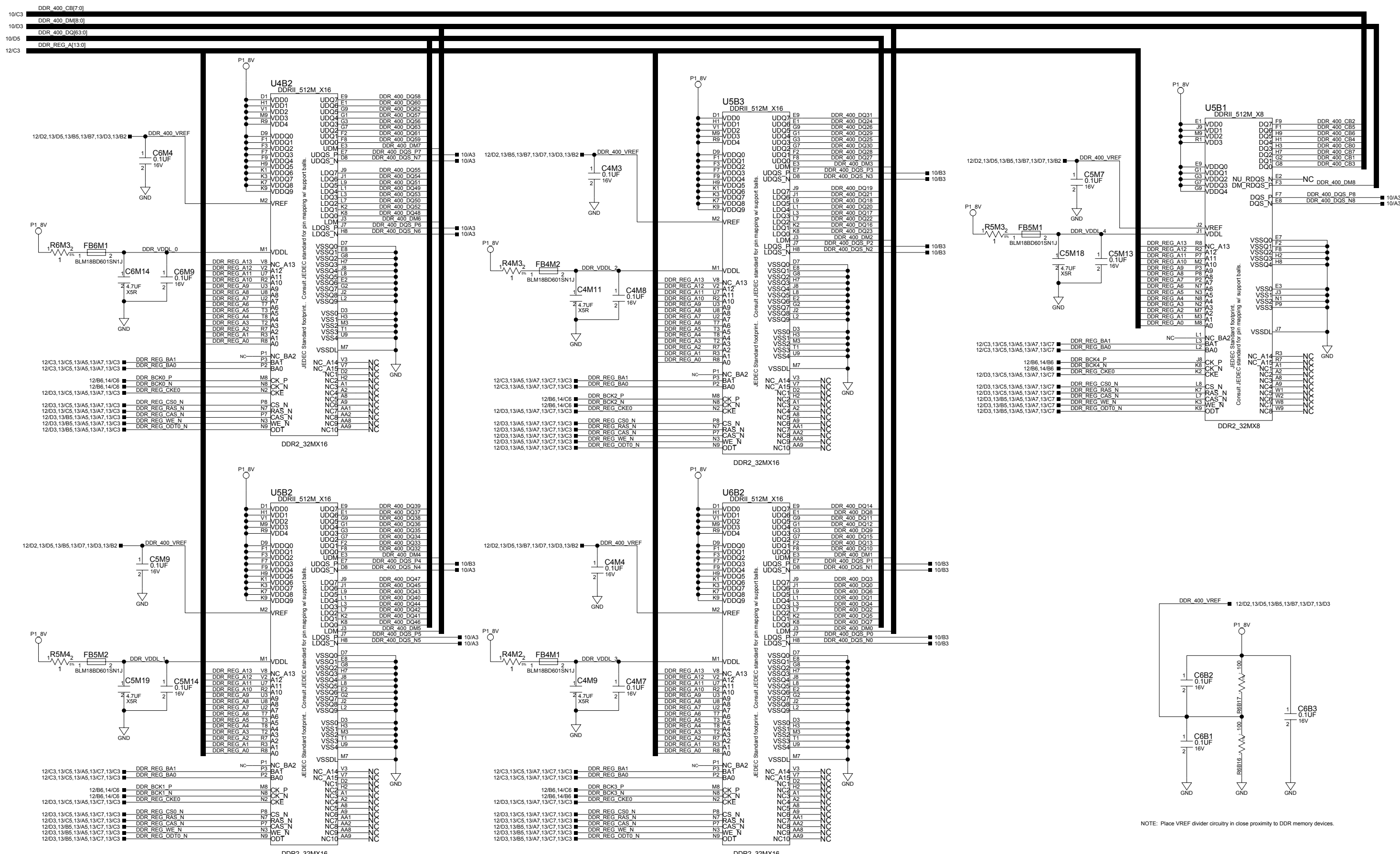
NOTE: Silkscreen YEL = LINK1000.

NOTE: Silkscreen as LINK10.



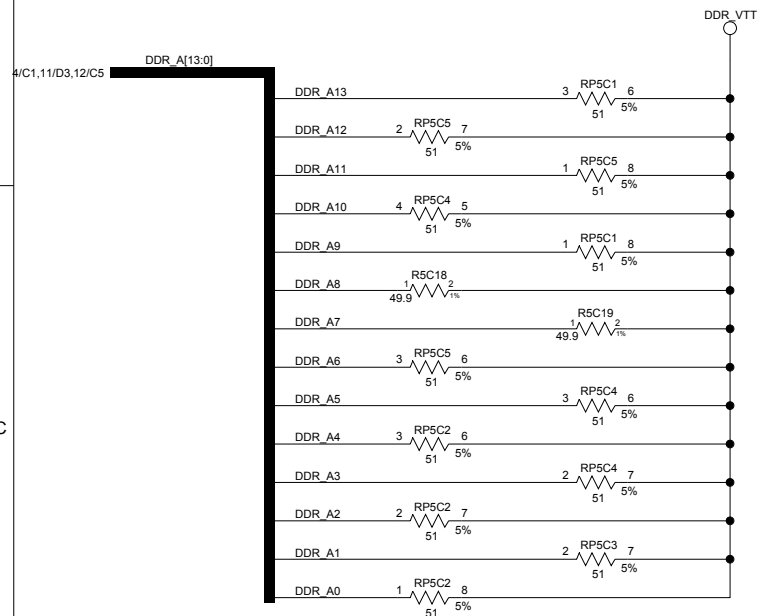




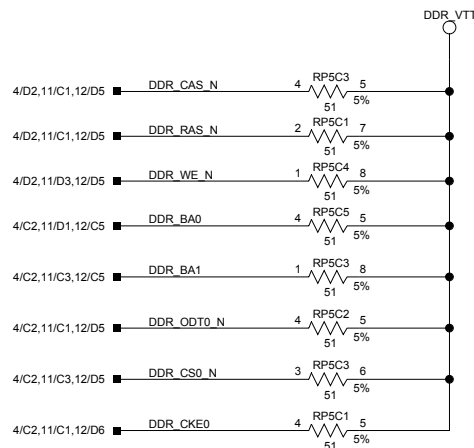
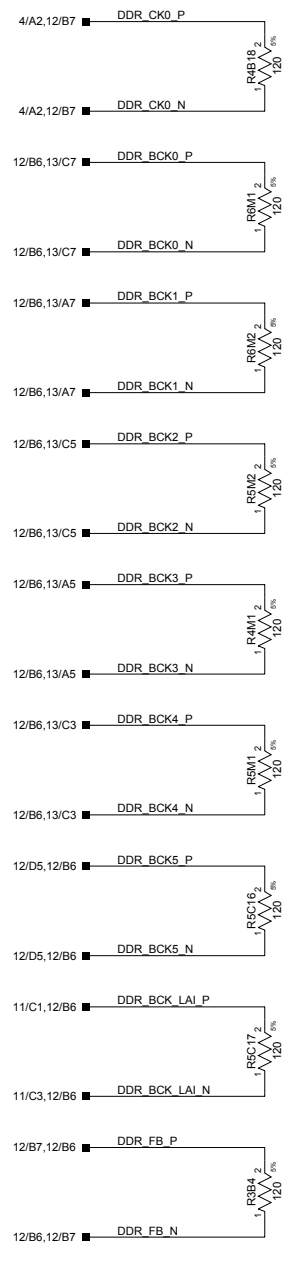


NOTE: Place VREF divider circuitry in close proximity to DDR memory devices.

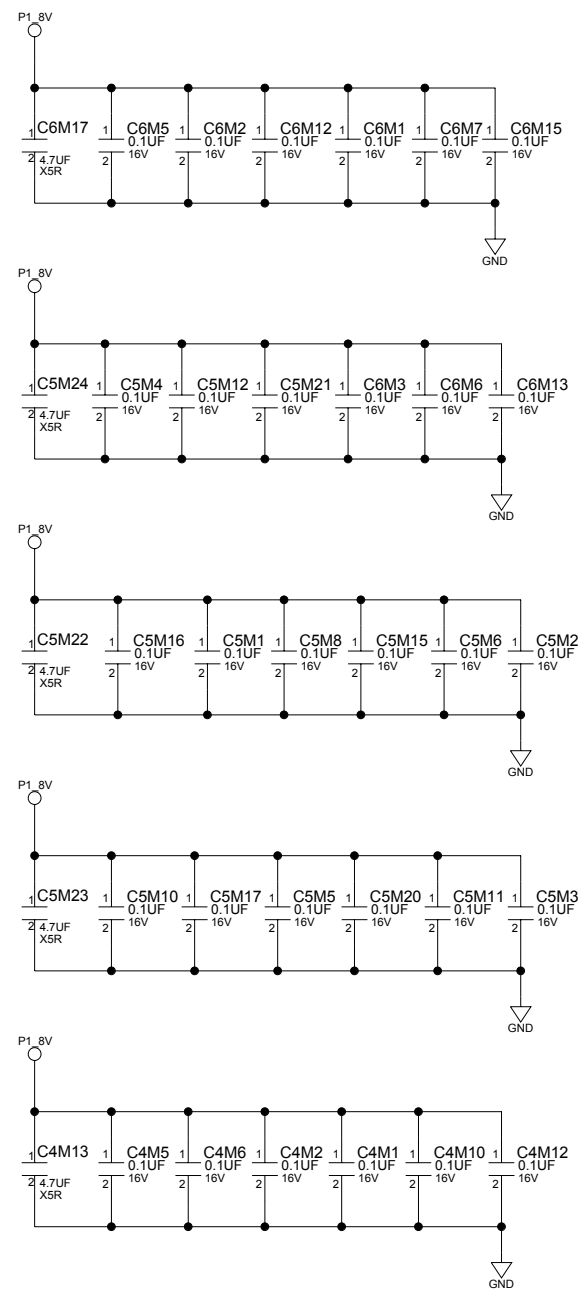
DDR VTT Termination



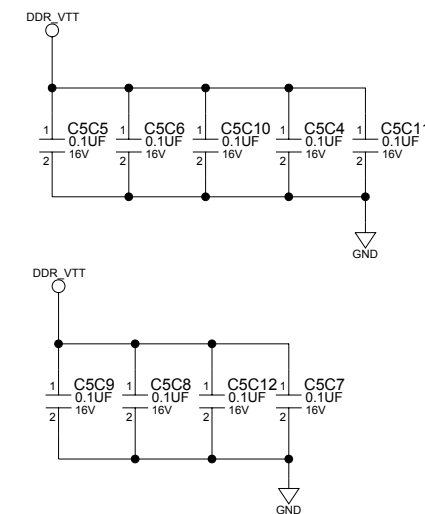
NOTE: Place termination as close to the input as possible.

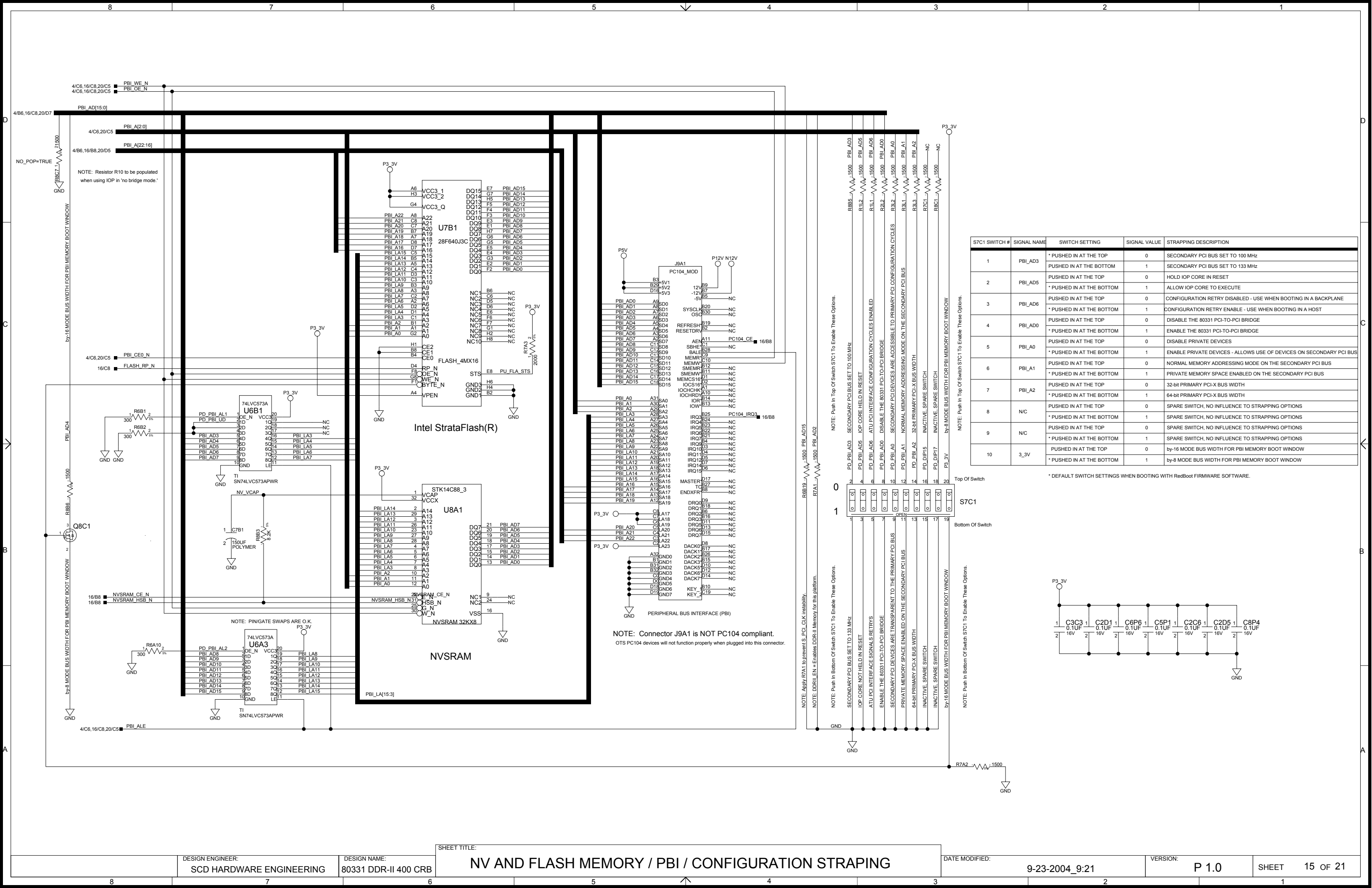


DDR VDD Decoupling



DDR VTT Decoupling



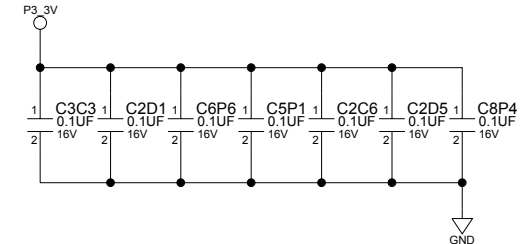


NOTE: Resistor R10 to be populated when using IOP in 'no bridge mode.'

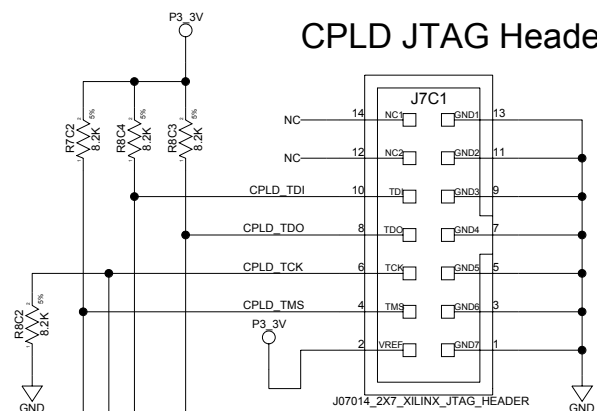
NOTE: Connector J9A1 is NOT PC104 compliant. OTS PC104 devices will not function properly when plugged into this connector.

S7C1 SWITCH #	SIGNAL NAME	SWITCH SETTING	SIGNAL VALUE	STRAPPING DESCRIPTION
1	PBI_AD3	* PUSHED IN AT THE TOP	0	SECONDARY PCI BUS SET TO 100 MHz
		PUSHED IN AT THE BOTTOM	1	SECONDARY PCI BUS SET TO 133 MHz
2	PBI_AD5	* PUSHED IN AT THE TOP	0	HOLD IOP CORE IN RESET
		* PUSHED IN AT THE BOTTOM	1	ALLOW IOP CORE TO EXECUTE
3	PBI_AD6	* PUSHED IN AT THE TOP	0	CONFIGURATION RETRY DISABLED - USE WHEN BOOTING IN A BACKPLANE
		* PUSHED IN AT THE BOTTOM	1	CONFIGURATION RETRY ENABLE - USE WHEN BOOTING IN A HOST
4	PBI_AD0	* PUSHED IN AT THE TOP	0	DISABLE THE 80331 PCI-TO-PCI BRIDGE
		* PUSHED IN AT THE BOTTOM	1	ENABLE THE 80331 PCI-TO-PCI BRIDGE
5	PBI_A0	* PUSHED IN AT THE TOP	0	DISABLE PRIVATE DEVICES
		* PUSHED IN AT THE BOTTOM	1	ENABLE PRIVATE DEVICES - ALLOWS USE OF DEVICES ON SECONDARY PCI BUS
6	PBI_A1	* PUSHED IN AT THE TOP	0	NORMAL MEMORY ADDRESSING MODE ON THE SECONDARY PCI BUS
		* PUSHED IN AT THE BOTTOM	1	PRIVATE MEMORY SPACE ENABLED ON THE SECONDARY PCI BUS
7	PBI_A2	* PUSHED IN AT THE TOP	0	32-bit PRIMARY PCI-X BUS WIDTH
		* PUSHED IN AT THE BOTTOM	1	64-bit PRIMARY PCI-X BUS WIDTH
8	N/C	* PUSHED IN AT THE TOP	0	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
		* PUSHED IN AT THE BOTTOM	1	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
9	N/C	* PUSHED IN AT THE TOP	0	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
		* PUSHED IN AT THE BOTTOM	1	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
10	3_3V	* PUSHED IN AT THE TOP	0	by-16 MODE BUS WIDTH FOR PBI MEMORY BOOT WINDOW
		* PUSHED IN AT THE BOTTOM	1	by-8 MODE BUS WIDTH FOR PBI MEMORY BOOT WINDOW

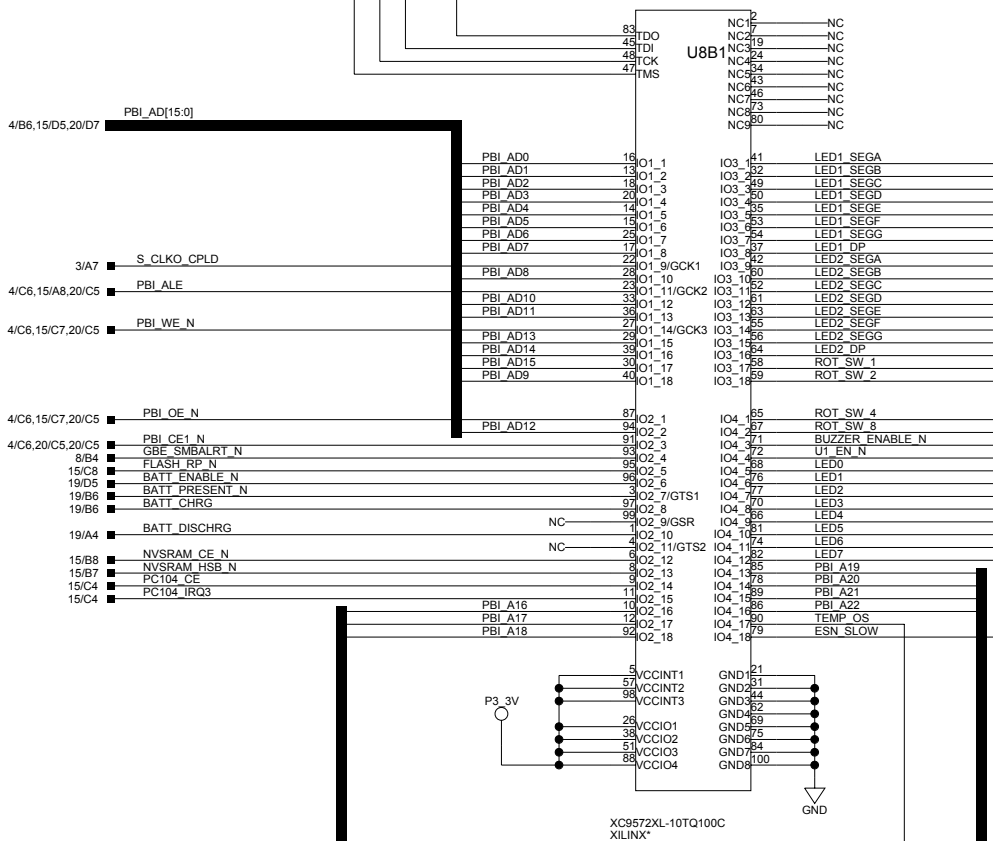
* DEFAULT SWITCH SETTINGS WHEN BOOTING WITH RedBoot FIRMWARE SOFTWARE.



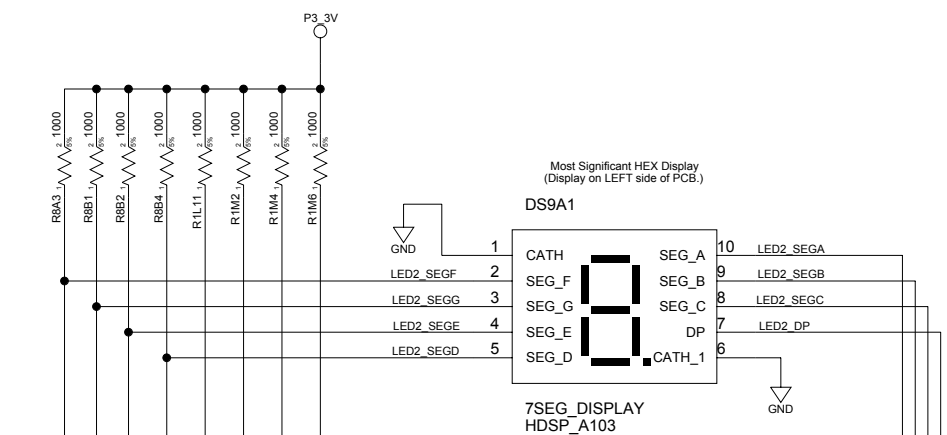
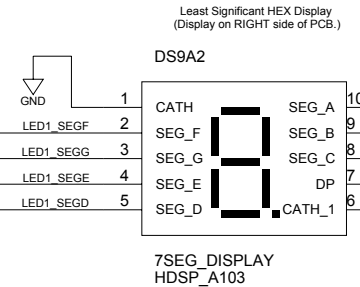
CPLD JTAG Header



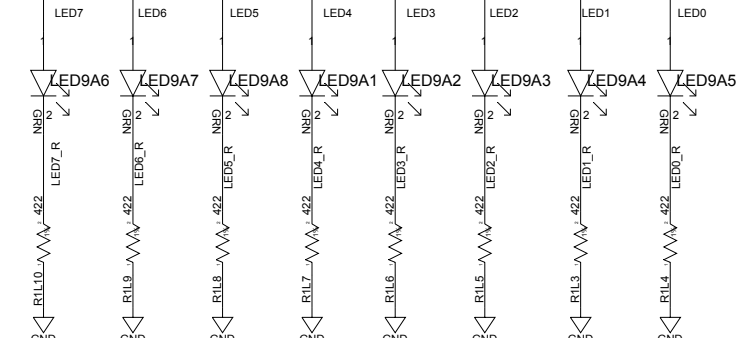
CPLD



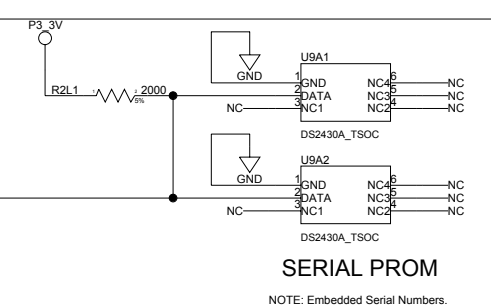
NOTE: When running RedBoot, a proper boot results with an output of A1 on hex display.
 NOTE: When core is held in reset (default setting), no output results on hex display.



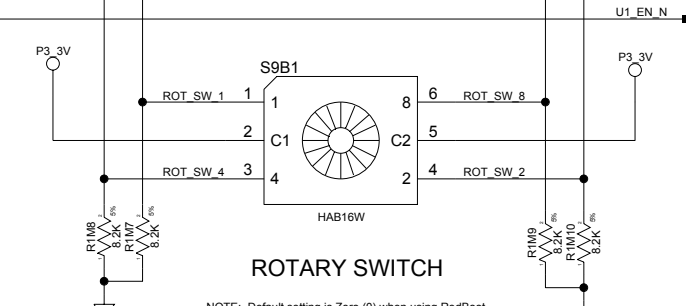
MISC. LEDS



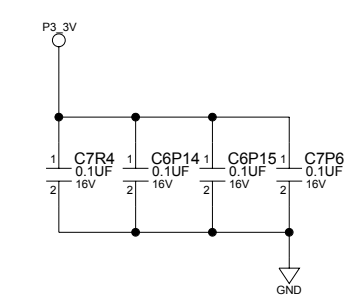
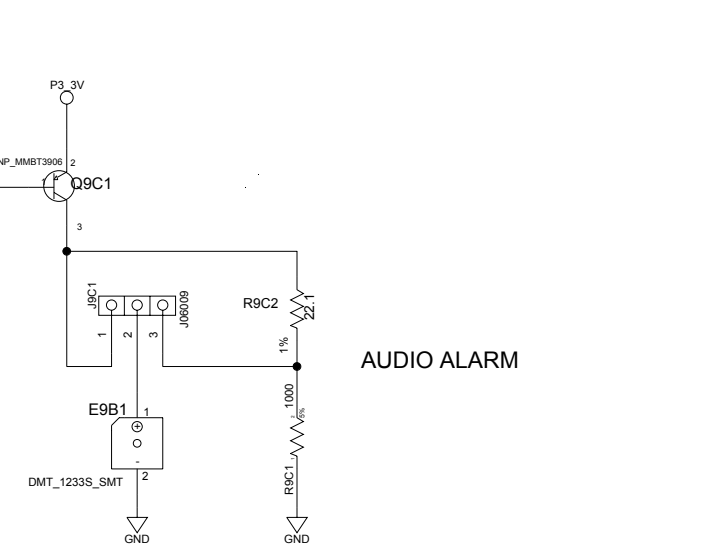
SERIAL PROM



ROTARY SWITCH



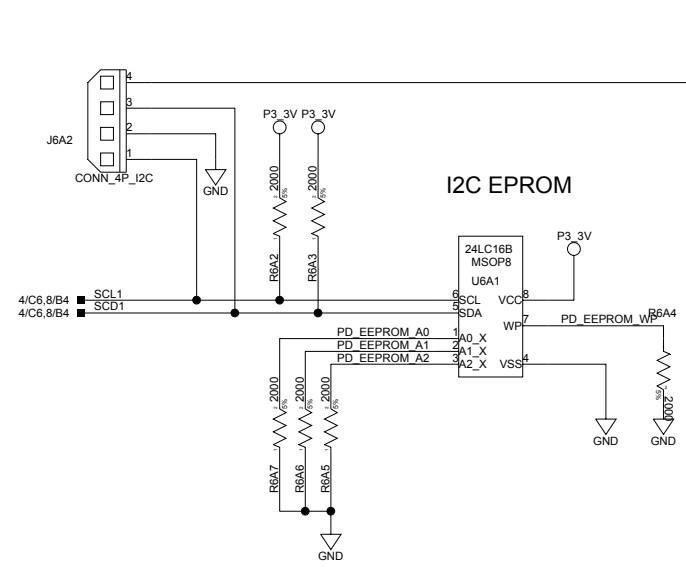
AUDIO ALARM



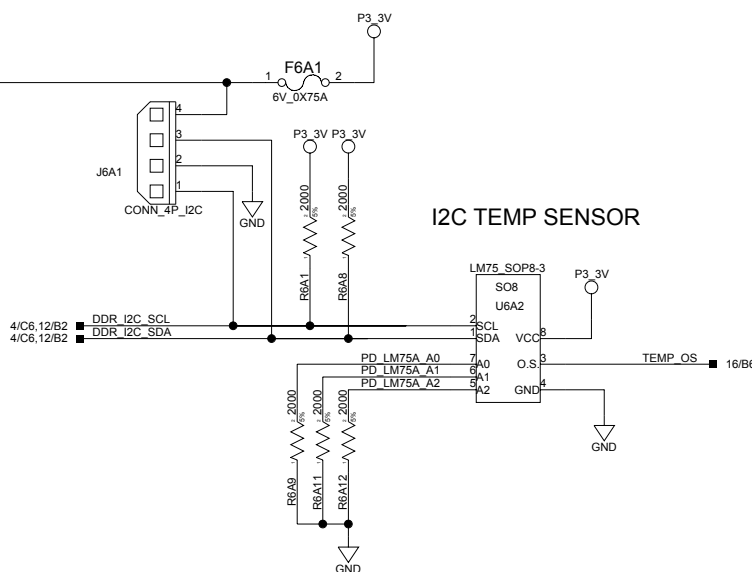
JUMPER J9C1

PINS	SETTINGS
N/C	Audio Alarm OFF
1 & 2	Audio Alarm LOUD
2 & 3	Audio Alarm QUIET

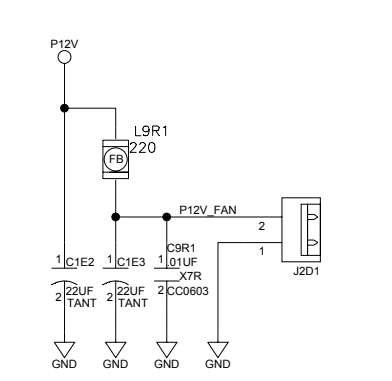
I2C EPROM HEADER



I2C TEMP SENSOR HEADER

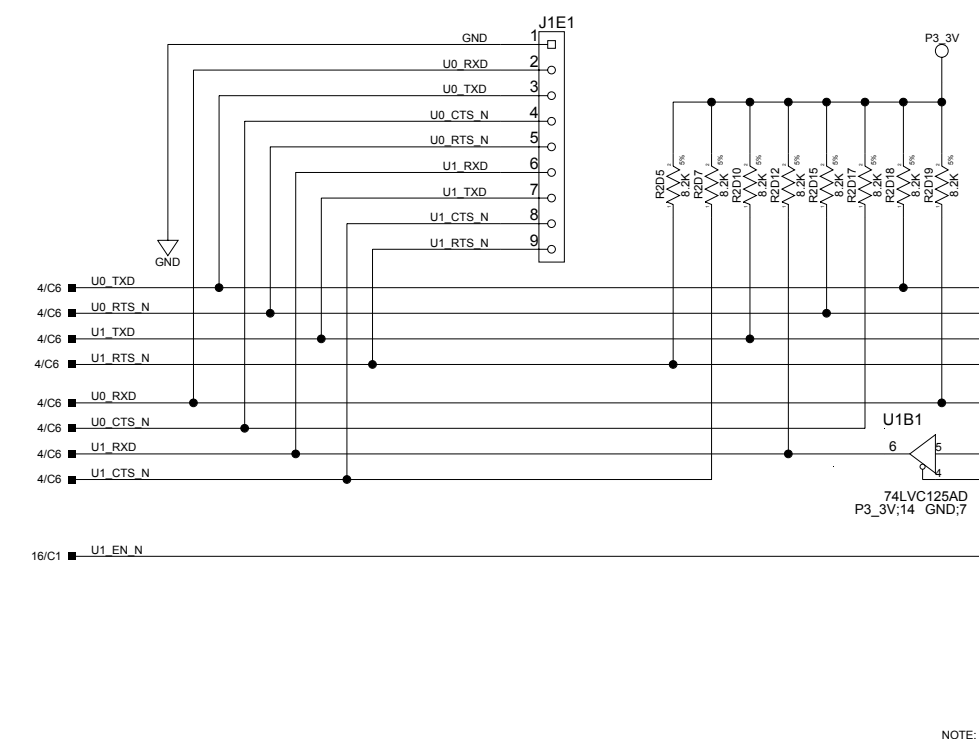


FAN POWER HEADER

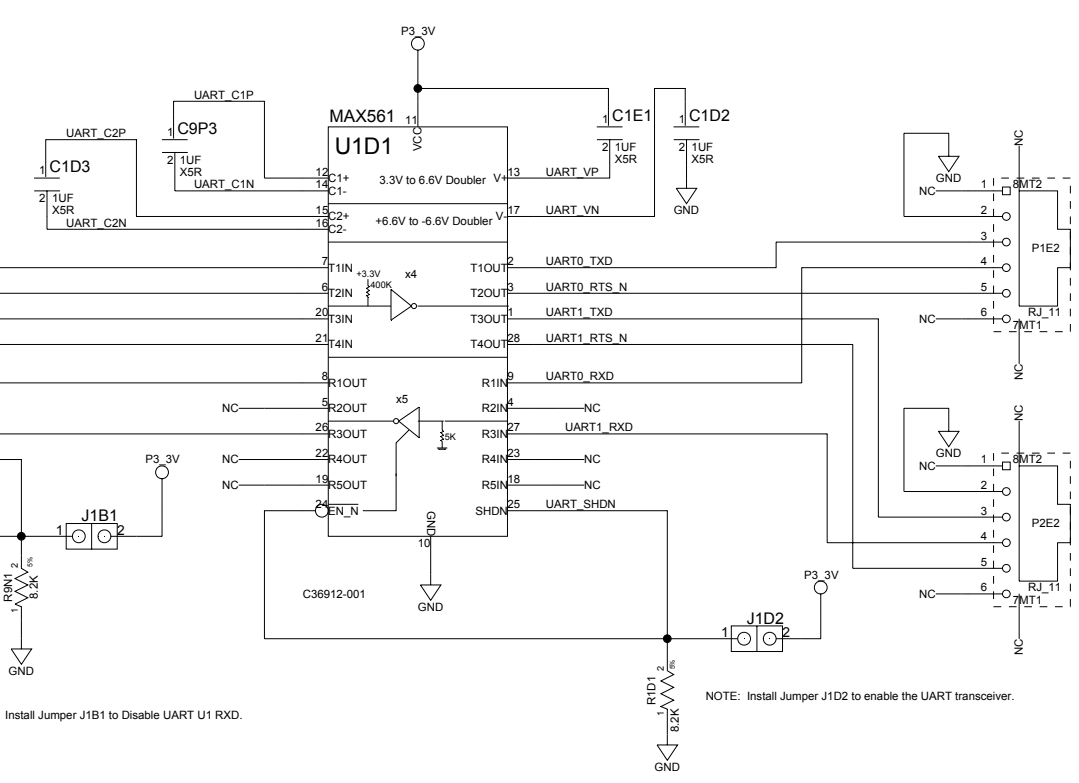


NOTE:
Header J2D1 is to be utilized for active IOP cooling.
The active heat sink part number is: C51829-001.
The passive IOP cooling solution requires at least 200 lfm across its surface.
The passive heat sink part number is: C50161-001.

UART HEADER



RS-232 TRANSCEIVER



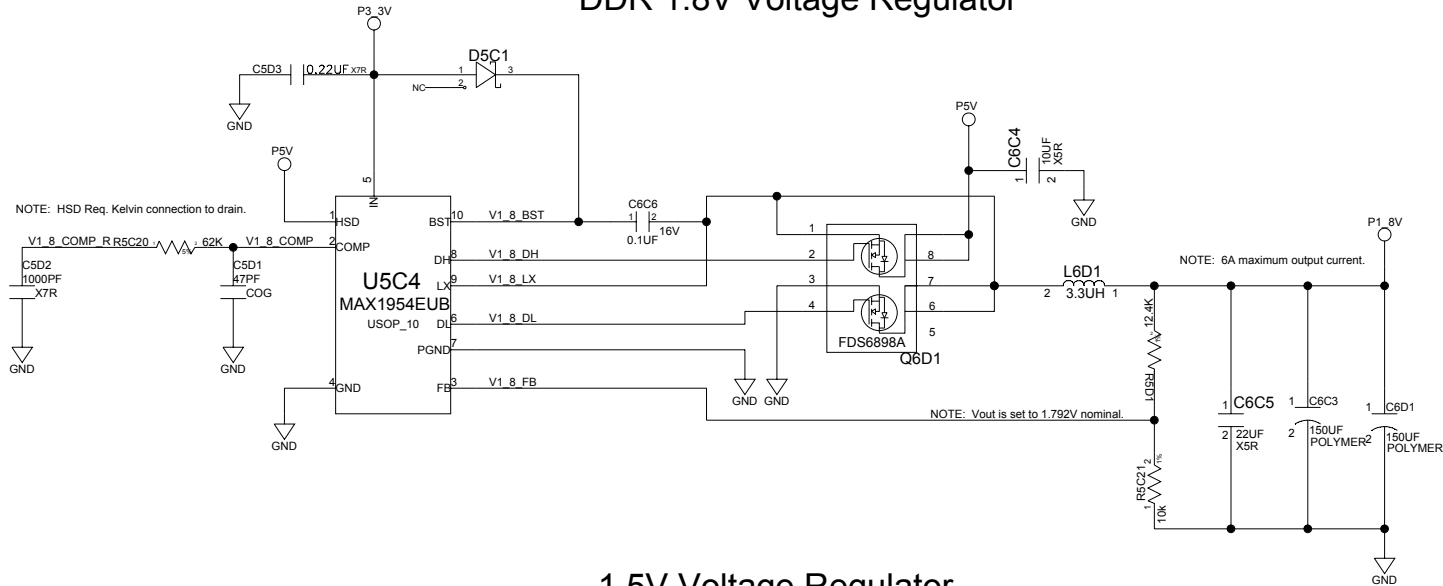
RJ11 Dual Serial Port Connector

NOTE: Lower RJ11 connector on PCB.
NOTE: Upper RJ11 connector on PCB.

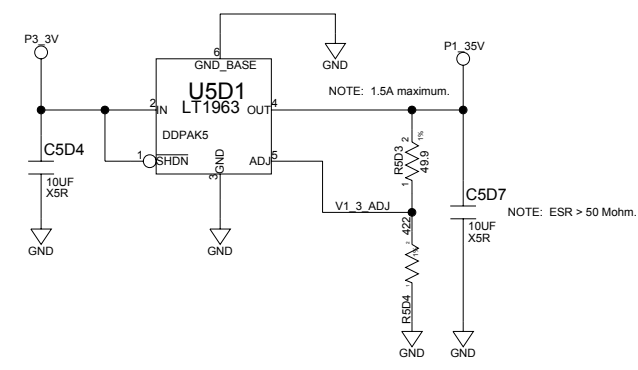
NOTE: Install Jumper J1B1 to Disable UART U1 RXD.

NOTE: Install Jumper J1D2 to enable the UART transceiver.

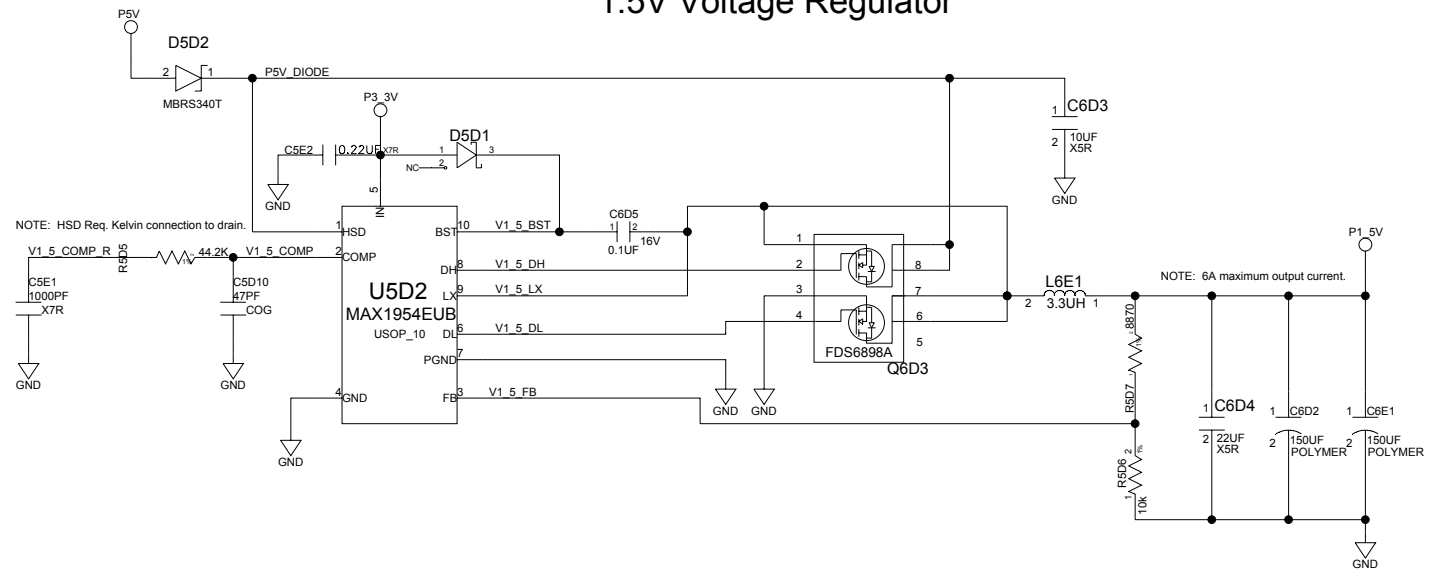
DDR 1.8V Voltage Regulator



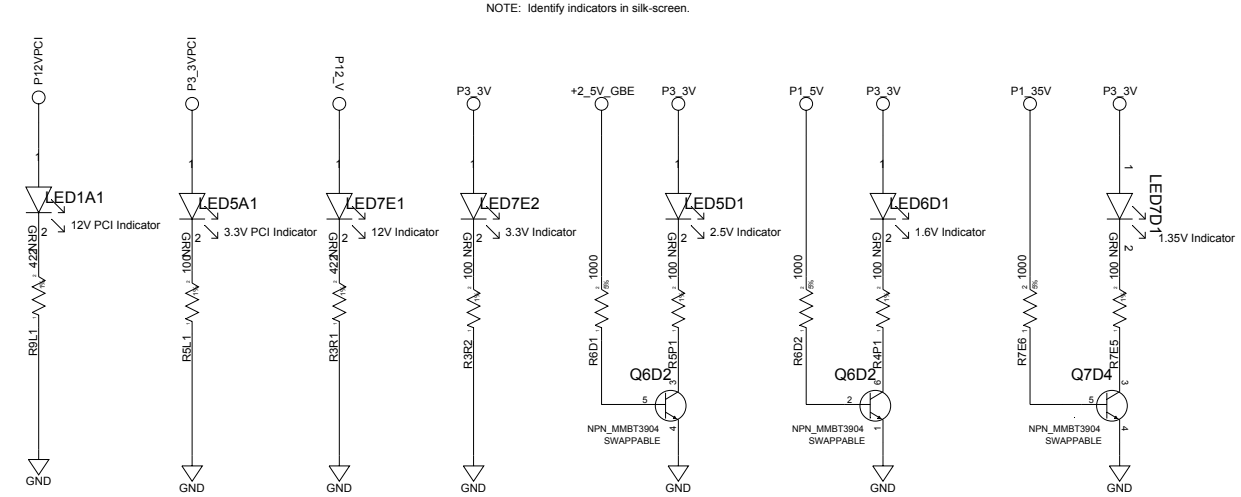
1.35V Voltage Regulator



1.5V Voltage Regulator

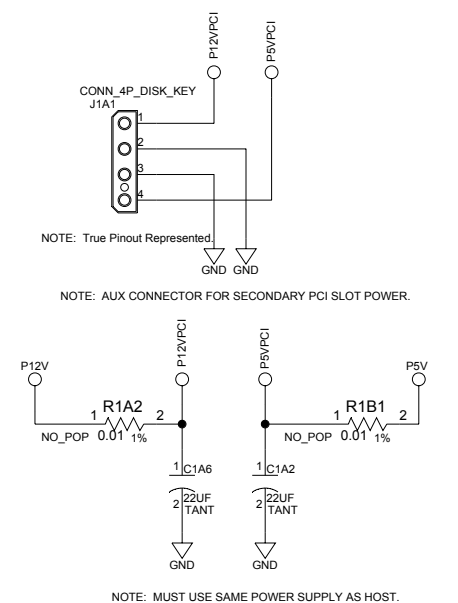


LED Indicators



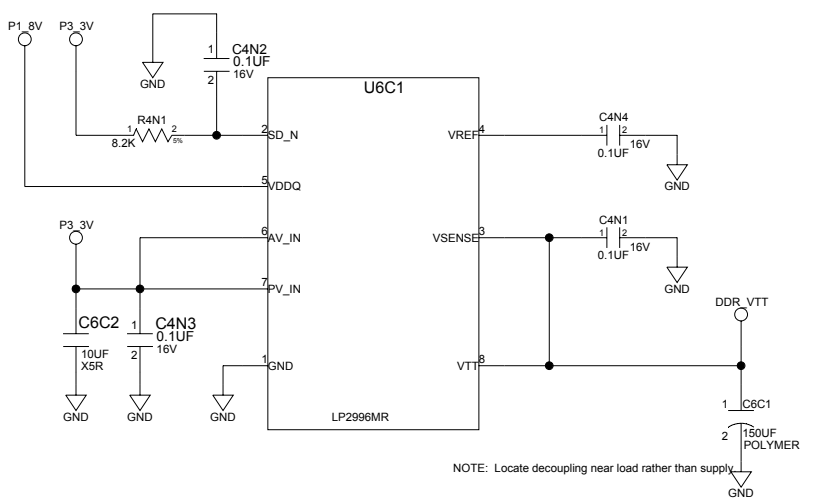
Secondary PCI-X Expansion Slot Power Connector

NOTE: Auxiliary power MUST be connected to use secondary PCI slot.

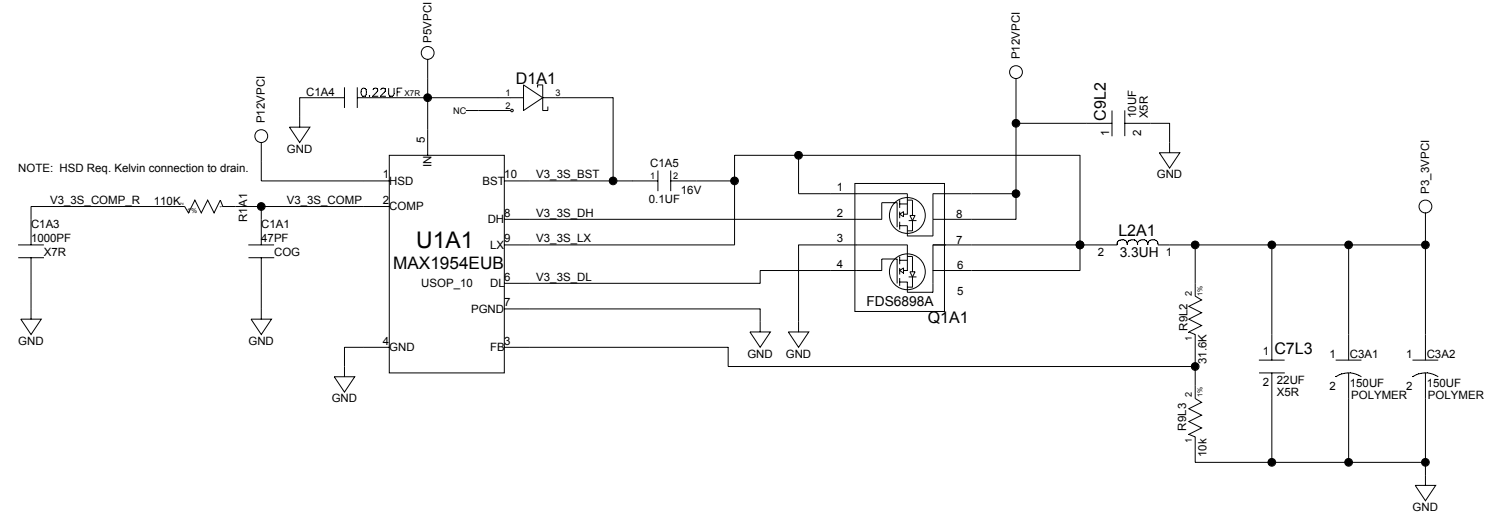


DDR VTT Voltage Regulator

NOTE: VREF powers up 150uS after +1.8V power rail.



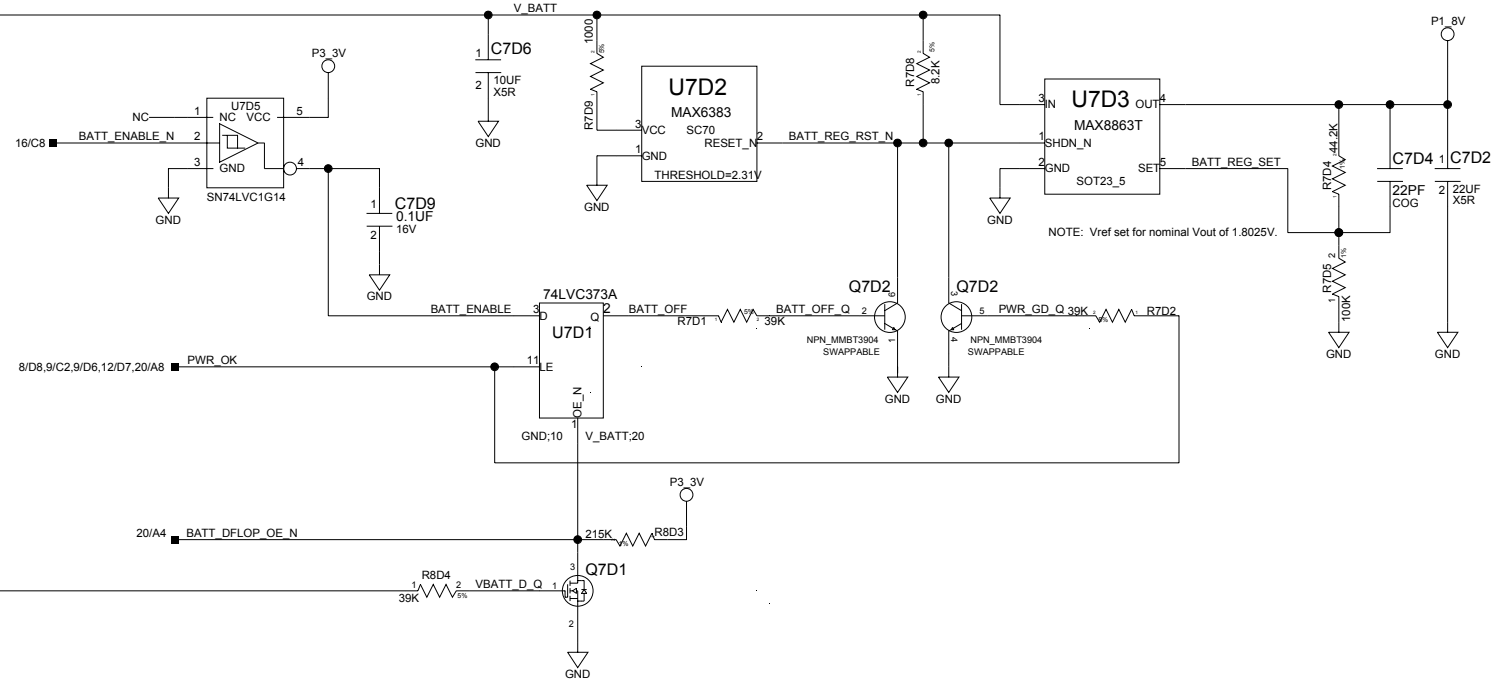
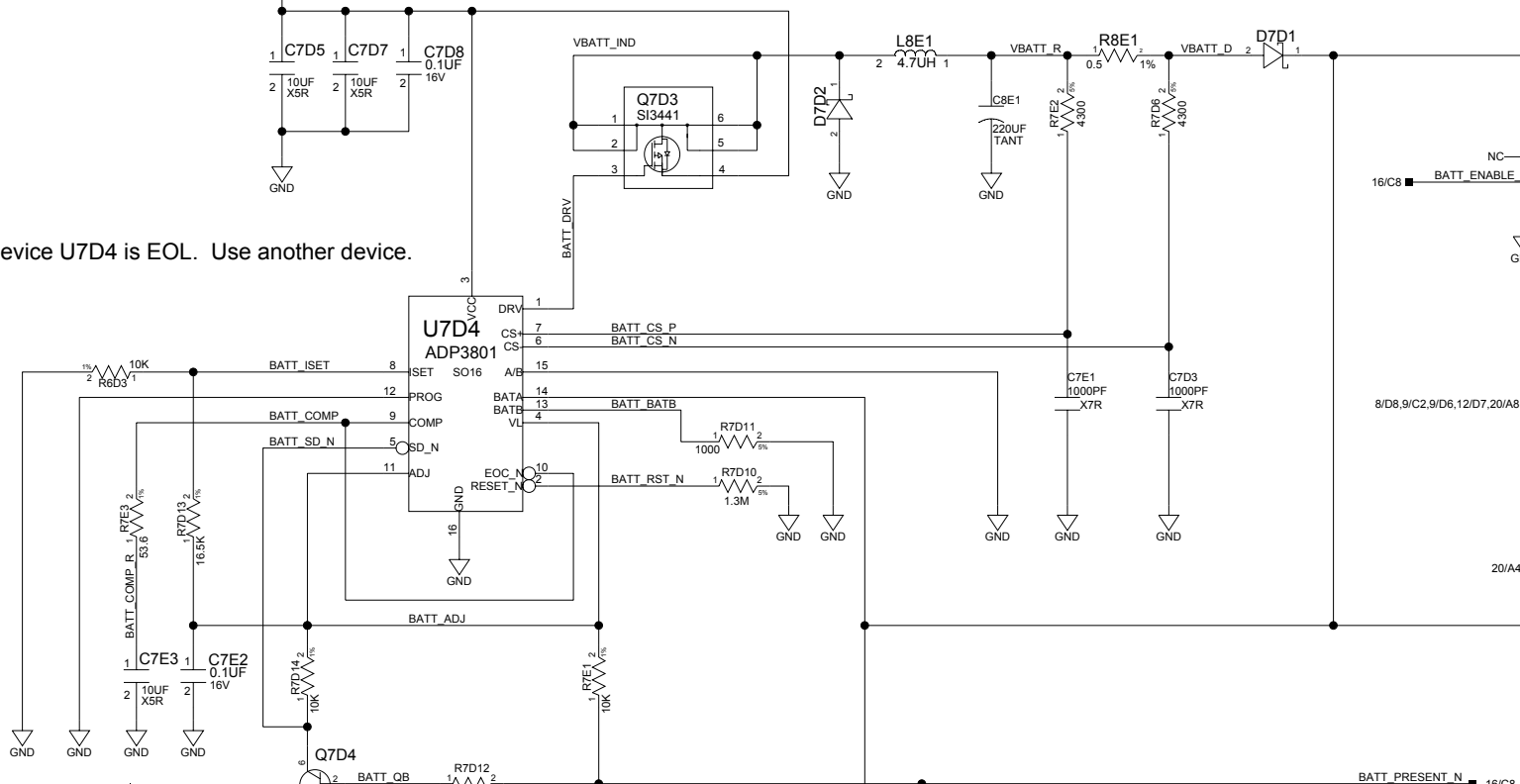
3.3V Voltage Regulator for PCI Slot



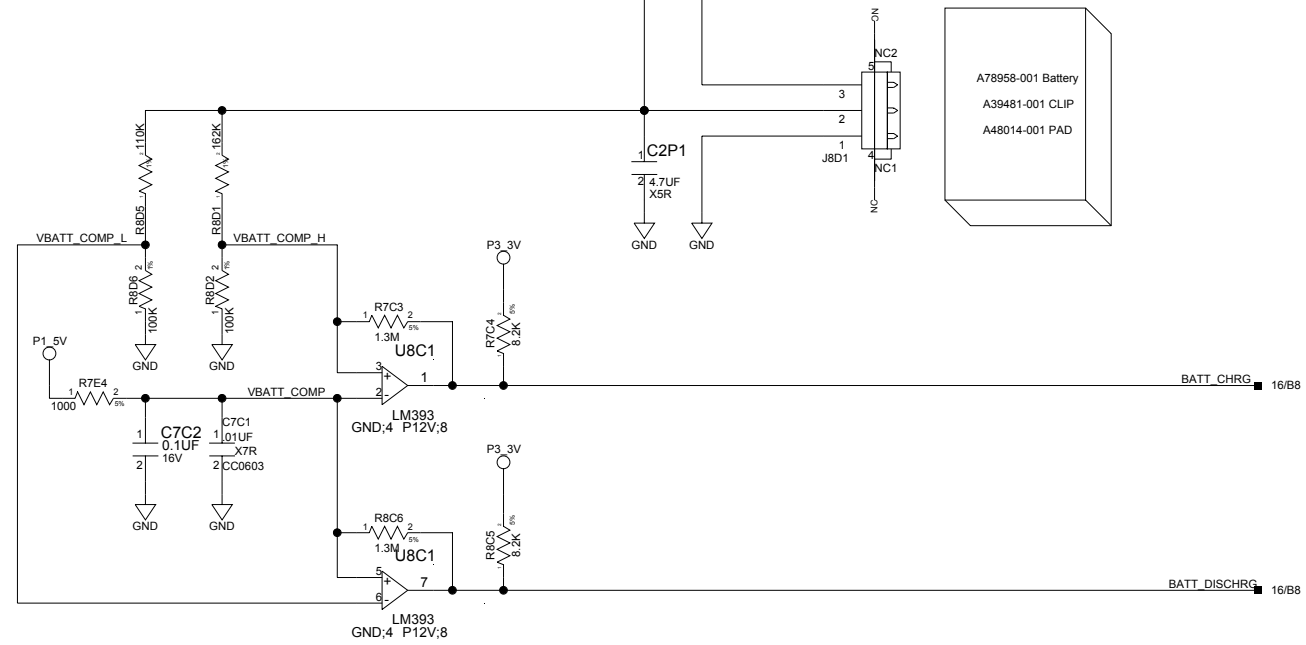
BATTERY BACKUP CONTROL CIRCUITRY

DDR SELF-REFRESH LINEAR REGULATOR

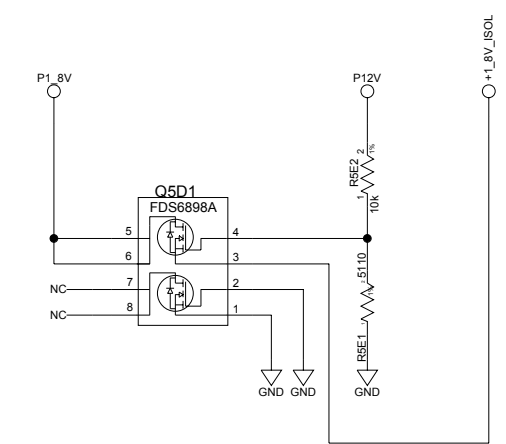
NOTE: Device U7D4 is EOL. Use another device.



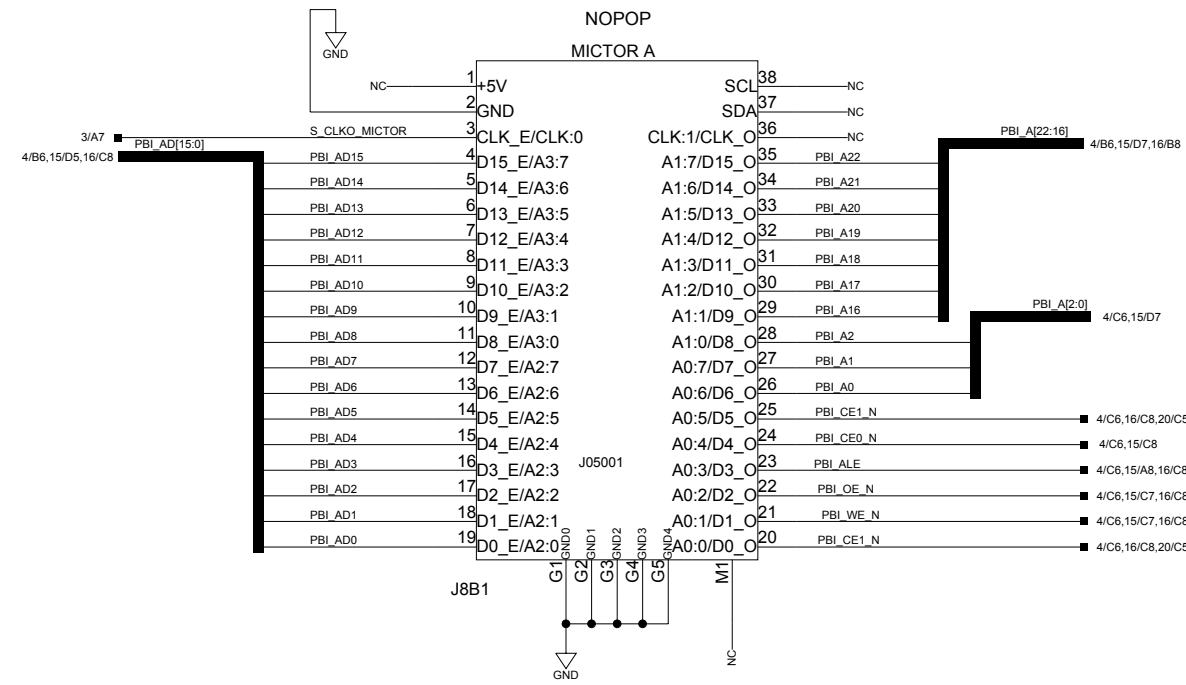
Battery Header



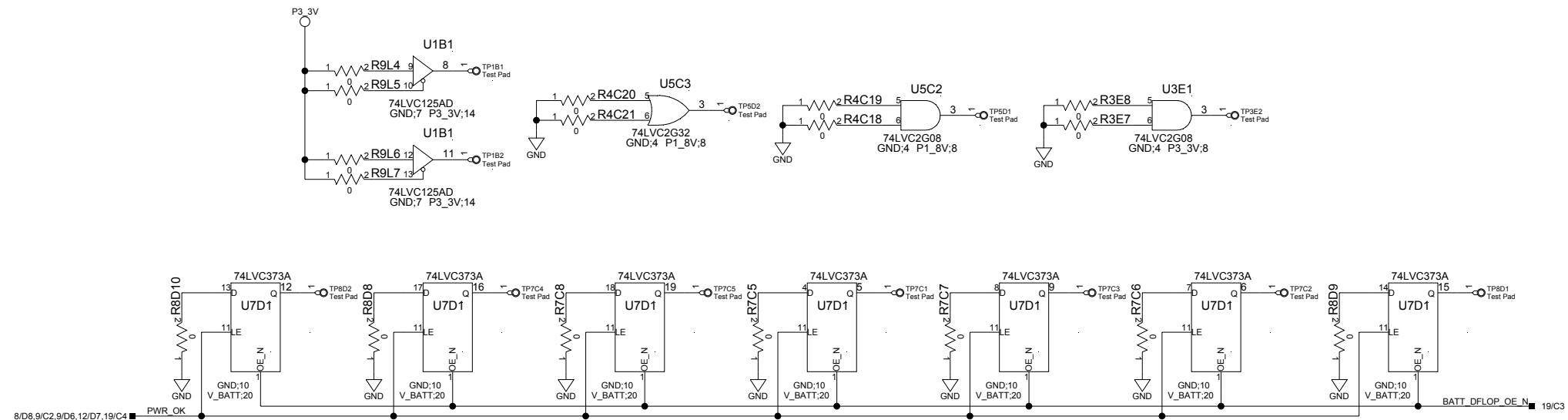
IOP 1.8V ISOLATION CIRCUITRY



DEBUG CONNECTOR



UNUSED PARTS



Version History

Ver 1.0 -- Proto Build 09/29/04