Intel® 80333 I/O Processor

Thermal Design Guidelines Application Note

May 2005

Document Number: 306630002US

Contents

Figures

Tables

Revision History

Date	Revision	Description
May 2005	002	Added ARM disclaimer to Legal page. Revised Table 1, Tcase from 105 to 95. Added Table 2, Note 1.
March 2005	001	Initial Release.

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1.0 Introduction

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heat sinks.

The purpose of this document is as follows:

- To specify the operating limits of the Intel® 80333 I/O Processor[1] (80333) component.
- To describe a reference thermal solution meeting thermal specifications for the 80333 component.

Properly designed thermal solutions provide adequate cooling to maintain the component die temperatures at or below thermal specifications. This is accomplished by providing a low local ambient temperature, ensuring adequate local airflow, and minimizing the die–to–local-ambient thermal resistance. By maintaining the component die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and can cause permanent changes in the operating characteristics of the component. The simplest and most cost-effective method is to improve the inherent system cooling characteristics through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions can be implemented in conjunction with system thermal solutions. The size of the fan or heat sink can be varied to balance size and space constraints with acoustic noise.

This document addresses thermal design and specifications for the components only. For thermal design information on other chipset components, refer to the datasheet of the respective component.

1.1 Definition of Terms

BGA	Ball Grid Array. A package type, defined by a resin-fiber substrate, onto which a die is mounted, bonded, and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
T_{case}	Maximum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.
TDP	Thermal Design Power. Thermal solutions must be designed to dissipate this target power level while keeping the die temperate under the maximum allowed.
T_J	Junction temperature
T_A	Ambient temperature
T_S	Sink temperature

1. Compliant with ARM* architecture

1.2 Reference Documents

The reader of this specification must also be familiar with the material and concepts presented in the following documents:

- *BGA/OLGA Assembly Development Guide*
- Various system thermal design suggestions located at http://www.formfactors.org.

Note: Unless otherwise specified, these documents are available through your Intel field sales representative. Some documents might not be available at this time.

2.0 Packaging Technology

The component uses a 37.5 mm × 37.5 mm, 10-layer FC-BGA package (Figure 1, Figure 2, and Figure 3).

Figure 1. Intel® 80333 I/O Processor Package Dimensions (Top View)

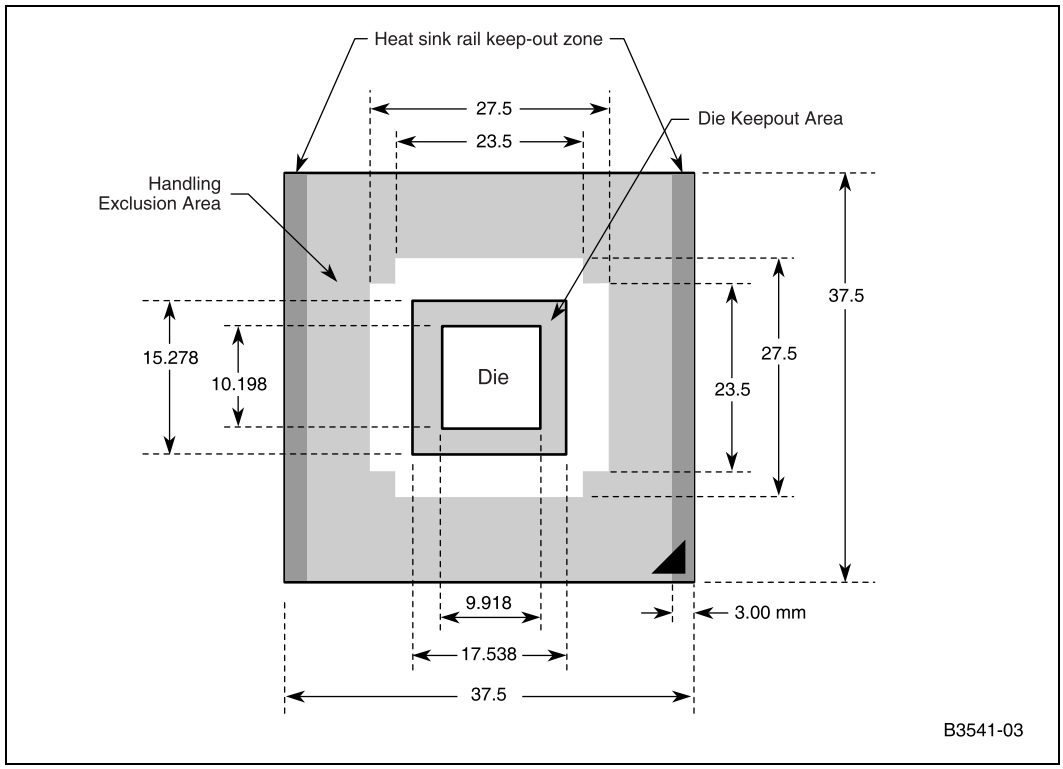


Figure 2. Package Dimensions (Side View)

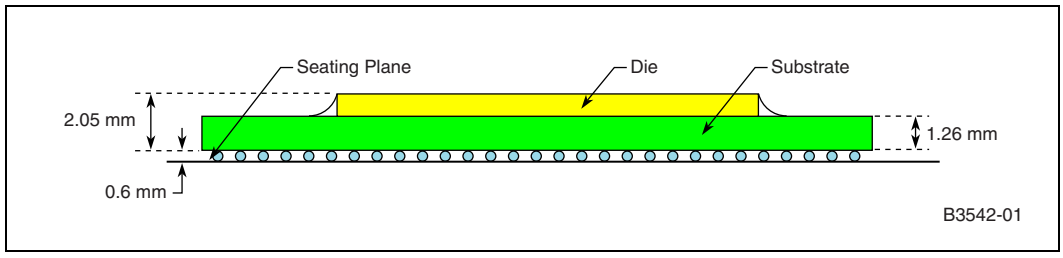
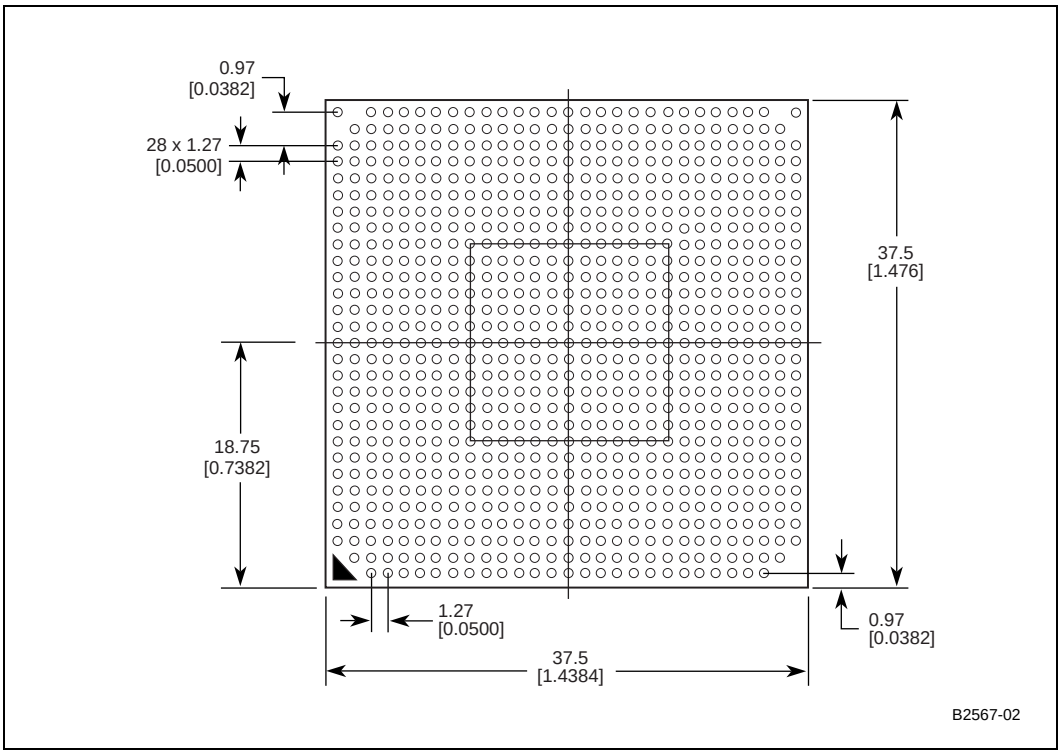


Figure 3. Package Dimensions (Bottom View)



3.0 Thermal Simulations

Intel provides thermal simulation models of the component and associated guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool "ICEPAK*" (version 4.0 or higher) by Fluent*. Contact your Intel field sales representative to order the thermal models and user's guides.

4.0 Thermal Specifications

4.1 Power

Flip Chip Ball Grid Array (FC-BGA) packages have poor heat-transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers plan for a heat sink when using this component. For Intel® 80333 I/O Processor power estimates, refer to the Icc characteristics (Table 24) in the *Intel® 80333 I/O Processor Datasheet*.

4.2 Die Temperature

To ensure proper operation and reliability of the component, the die temperatures must be at or below the values specified in Table 1. System- and/or component-level thermal solutions are required to maintain die temperatures below the maximum temperature specifications. Refer to Section 5.0, "Thermal Metrology" on page 12 for guidelines on accurately measuring package die temperatures.

Table 1. Intel® 80333 I/O Processor Thermal Specifications

Device	T_{case} (°C)	T_J max (°C)	$P_{THERMAL}$ (W)
Intel® 80333 I/O Processor	95	110	10.94[1]

NOTE:
1. This is the expected worst-case power used to calculate reference thermal solution.

5.0 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the die temperatures. Section 5.1 provides guidelines on how to accurately measure the die temperatures.

5.1 Die Temperature Measurements

To ensure functionality and reliability, the T_{case} of the Intel® 80333 I/O Processor must be maintained at or below the maximum temperature specification as noted in Table 1. The surface temperature at the geometric center of the die corresponds to T_{case}. Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors can be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heat sink base (when a heat sink is used). To maximize measurement accuracy, only the 0° thermocouple attach approach is recommended.

5.1.1 Zero-Degree Angle Attach Methodology

1. Mill a hole 3.3 mm (0.13 in.) in diameter and 1.5 mm (0.06 in.) deep, centered on the bottom of the heat sink base.
2. Mill a slot 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep from the centered hole to one edge of the heat sink. The slot must be parallel to the heat sink fins (Figure 4).
3. Attach thermal interface material (TIM) to the bottom of the heat sink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts must match the slot and hole milled into the heat sink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heat sink base, because any contact will affect the thermocouple reading. It is critical that the thermocouple bead makes contact with the die (Figure 5).
6. Attach heat sink assembly to the 80333 and route thermocouple wires out through the milled slot.

Figure 4. Zero-Degree Angle Attach Heat Sink Modifications

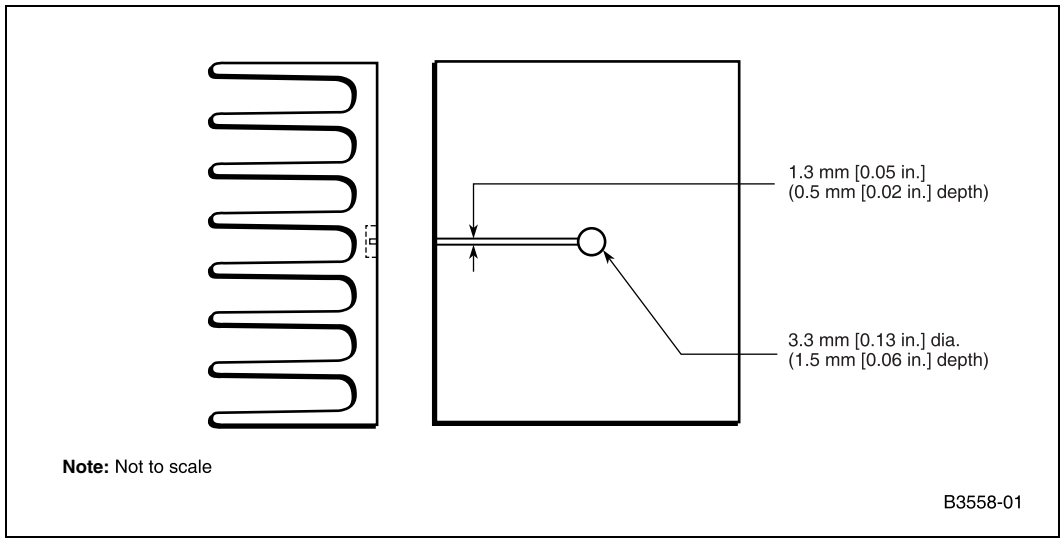
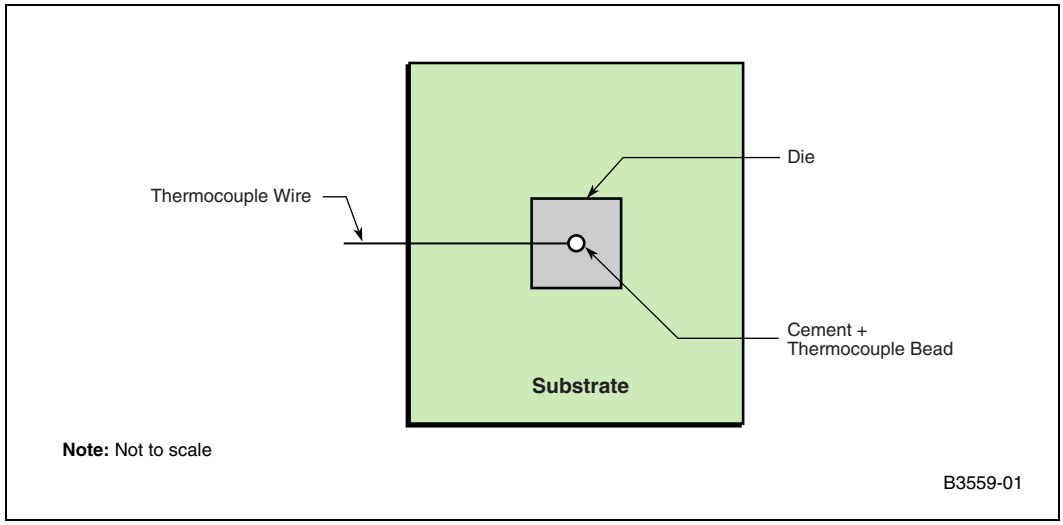


Figure 5. Zero-Degree Angle Attach Methodology (Top View)



6.0 Reference Thermal Solution

Intel has developed a reference thermal solutions designed to meet the cooling needs of the component under worst-case conditions. This section describes the overall requirements for the reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components might or might not need attached thermal solutions, depending on your specific system local-ambient operating conditions.

6.1 Operating Environment

The reference thermal solution was designed assuming a maximum local-ambient temperature of 50 °C at an elevation of 1800 m. The minimum recommended airflow velocity at the heat sink is 200 linear feet per minute (LFM) measured from the heat sink center. The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate.

6.2 Heat Sink Performance

This section is supplied with a measured thermal performance of the heat sink solution versus airflow rate.

Table 2. Heat Sink Performance Data

Air Flow (LFM)	ψ_{SA} (18 °C @ Sea Level)	ψ_{SA} (50 °C @ 1800 m)	θ_{JS} EOLine (°C/W)	θ_{JA} EOLine (°C/W)
100[1]	4.38	5.35	0.67	6.01
200	3.56	4.34	0.67	5.01
300	3.15	3.84	0.67	4.51

1. The minimum recommended airflow is 200 LFM, as stated in Section 6.1. This table includes 100 LFM only as a reference point.

Equation 1. Heat Sink Performance Equations

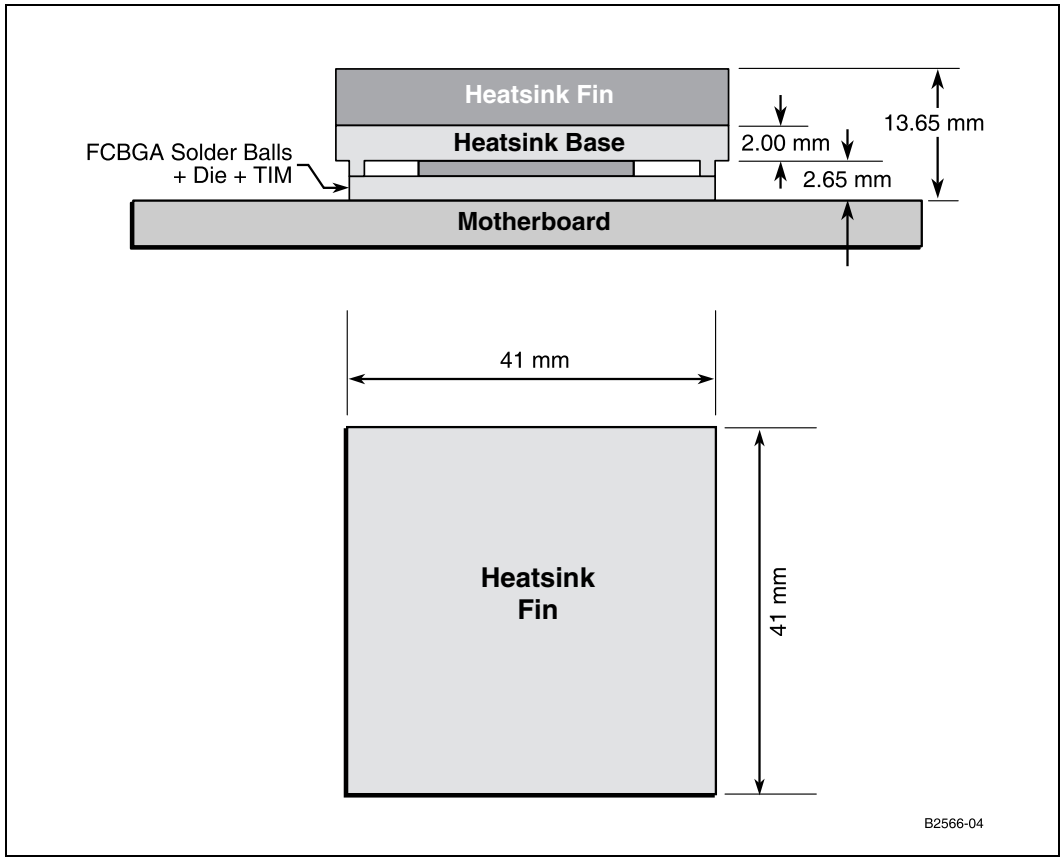
$$\Psi_{SA} = \frac{T_S - T_A}{P} \qquad \Theta_{JS} = \frac{T_J - T_S}{P} \qquad \Theta_{JA} = \Psi_{SA} + \Theta_{JS}$$

NOTES:
1. T_S = Heat sink temperature
2. T_A = Ambient temperature
3. P = Die power
4. θ_{JS} = TIM thermal resistance denotes the TIM performance
5. ψ_{SA} = Heat sink to ambient thermal resistance denotes the heat sink performance
6. θ_{JA} = Package to ambient thermal resistance

6.3 Mechanical Design Envelope

Although each design can have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the thermal solution are shown in Figure 6. When using heat sinks that extend beyond the reference heat sink envelope shown in Figure 6, any motherboard components placed between the heat sink and motherboard cannot exceed 2.65 mm (0.110 in.) in height.

Figure 6. Intel® 80333 I/O Processor Heat Sink Clip Volumetric Envelope for the Component



6.4 Keep-Out Dimensions of the Board-Level Components

The locations of hole patterns and keep-out zones for the reference thermal solution are shown in Figure 7 and Figure 8.

6.5 Heat Sink Clip Thermal Solution Assembly

The reference thermal solution for the component is a passive extruded heat sink with thermal interface. It is attached using a four-leg clip with four hooks directly penetrating through board holes and firmly engaged to the secondary side of the board. Figure 9 shows the reference thermal solution assembly and associated components. Full mechanical drawings of the thermal solution assembly and the heat sink clip are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

Figure 7. Intel® 80333 I/O Processor Heat Sink Clip Board Component Keep-Out Zones

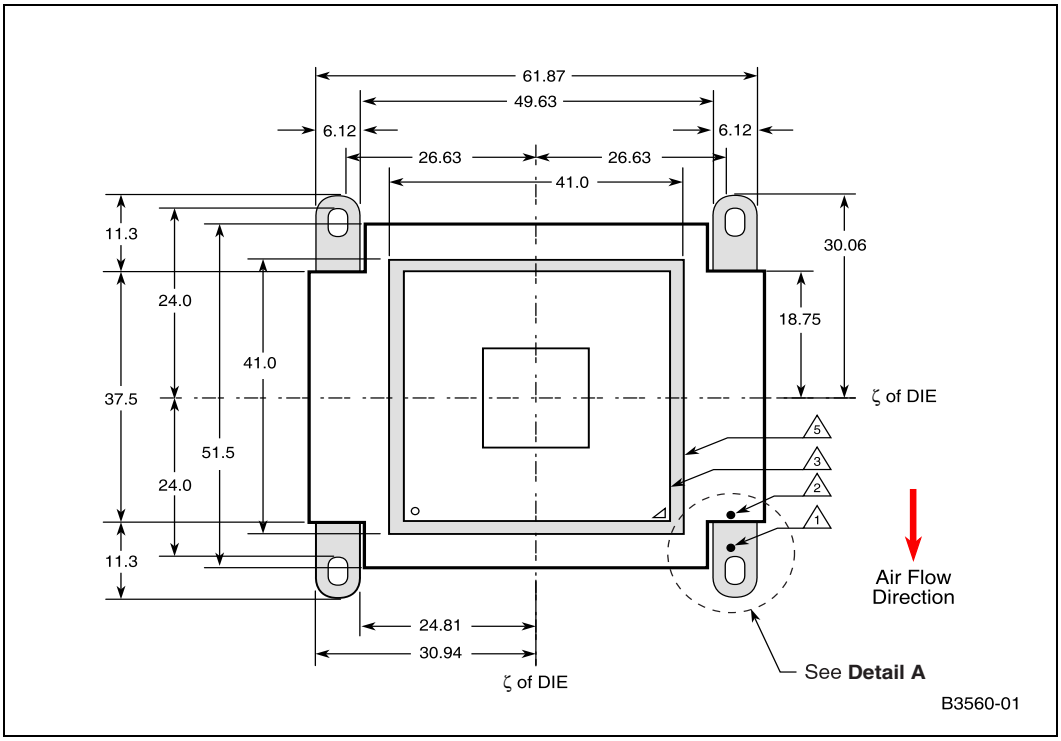
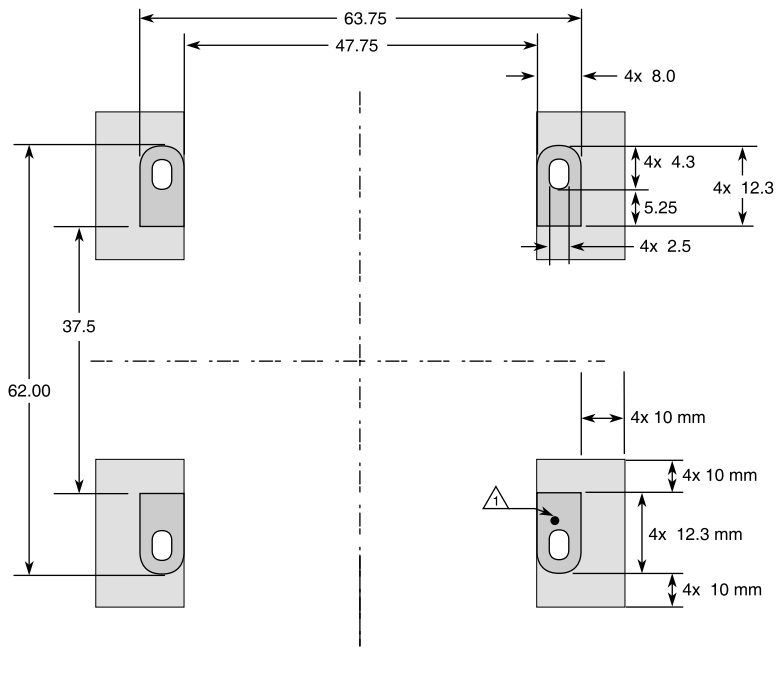


Figure 8. Intel® 80333 I/O Processor Retention Mechanism Component Keep-Out Zones

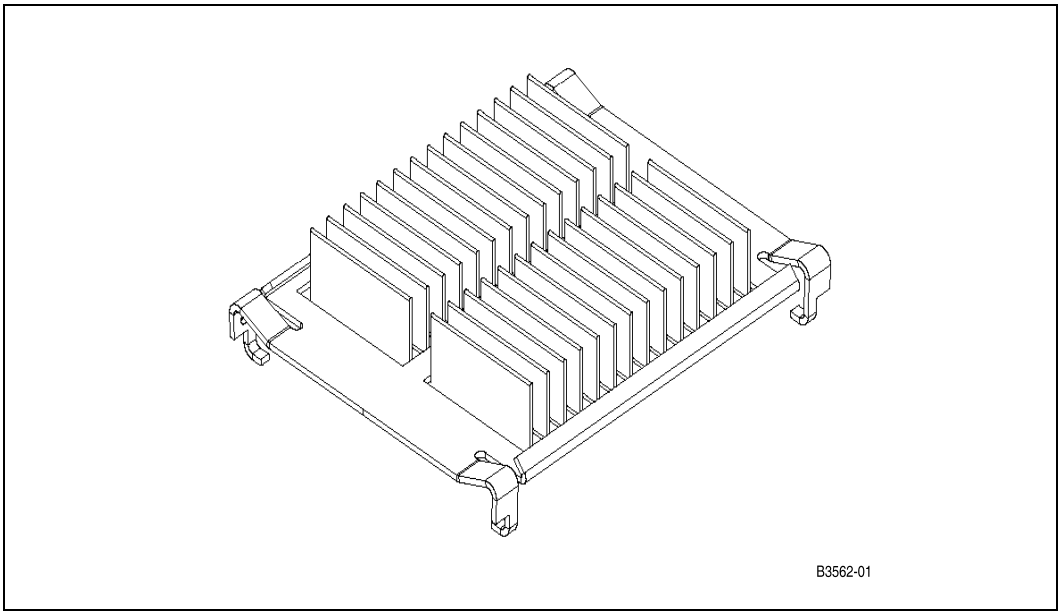


- The purpose of the Keep-Out Zone (KOZ) is to avoid hand-tool interference with the placement of adjacent components.
- The assembly KOZ was added to the existing retention mechanism KOZ. Refer to the Intel reference hand-tool design shown in Figure 11 on page 20.
- The assembly KOZ might change if customers apply their own installation hand-tool design.

6.5.1 Heat Sink Orientation

Since this solution is based on a unidirectional heat sink, the mean airflow direction must be aligned with the direction of the fins of the heat sink.

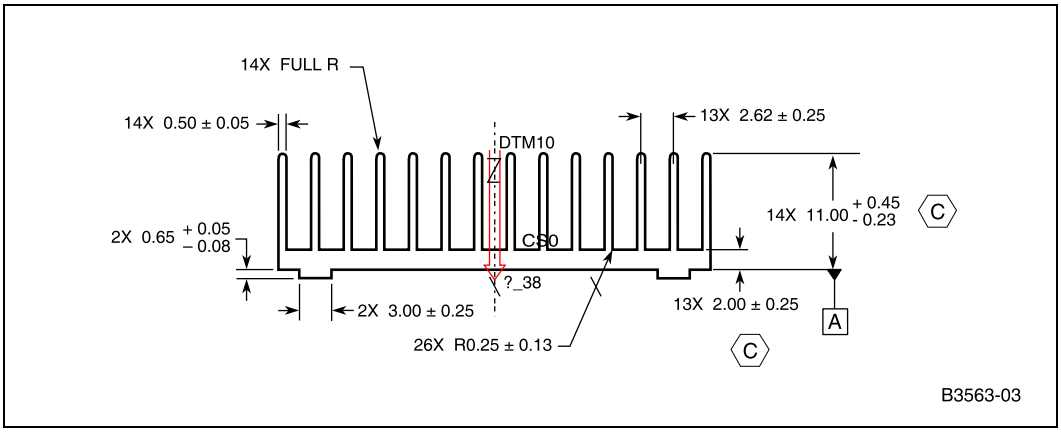
Figure 9. Intel® 80333 I/O Processor Heat Sink Clip Assembly



6.5.2 Extruded Heat Sink Profiles

The reference heat sink clip uses an extruded heat sink for cooling the component. Figure 10 shows the heat sink profile. Appendix A lists a supplier for this extruded heat sink. Other heat sinks with similar dimensions and increased thermal performance might be available. Full mechanical drawing of this heat sink is provided in Appendix B.

Figure 10. Intel® 80333 I/O Processor Heat Sink Extrusion Profile



6.5.3 Mechanical Interface Material

There is no mechanical interface material associated with this reference solution.

6.5.4 Thermal Interface Material

A thermal interface material provides improved conductivity between the die and the heat sink. The reference thermal solution uses Honeywell* PCM45HD, 0.0508 mm (0.002 in.) thick, 20 mm × 20 mm (0.7874016 in. × 0.7874016 in.) square.

Alternate reference thermal solution recommended is PCM45F.

6.5.4.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). The effect of pressure on the thermal resistance of the Honeywell* PCM45HD TIM can be found at the following URL:

http://www.honeywell.com/sites/sm/em/interpack.htm

The heat sink clip provides enough pressure for the TIM to achieve a thermal conductivity of 0.2 × C cm^2/W (5.0 W/m × C).

6.5.5 Heat Sink Clip

The reference solution uses a clip with hooked ends. The hooks penetrate through the board holes and are firmly engaged to the secondary side of the board. See Appendix B for a mechanical drawing of the clip.

6.5.6 Heat Sink Clip Assembly

It is recommended to use a hand tool to ease the heat sink clip assembly, with support fixture, beneath the package to be assembled. The support fixture is used to provide support to the package, in order to reduce the board deflection on the BGA solder ball. Figure 11 shows the recommended hand-tool design. The hand tool consist of the handle and metal groove. The groove is designed in the metal, in order to be inserted into the leg of the clip, so as to ease the bending and pressing process of the heat sink clip assembly. Figure 12 shows the heat sink clip assembly with groove inserted into the leg of the clip.

It is also recommended that the die on the package is cleaned with isopropyl alcohol (IPA) prior to the heat sink clip assembly. This is to ensure the thermal interface material (TIM) functions per the specification.

Figure 11. Hand-Tool Design

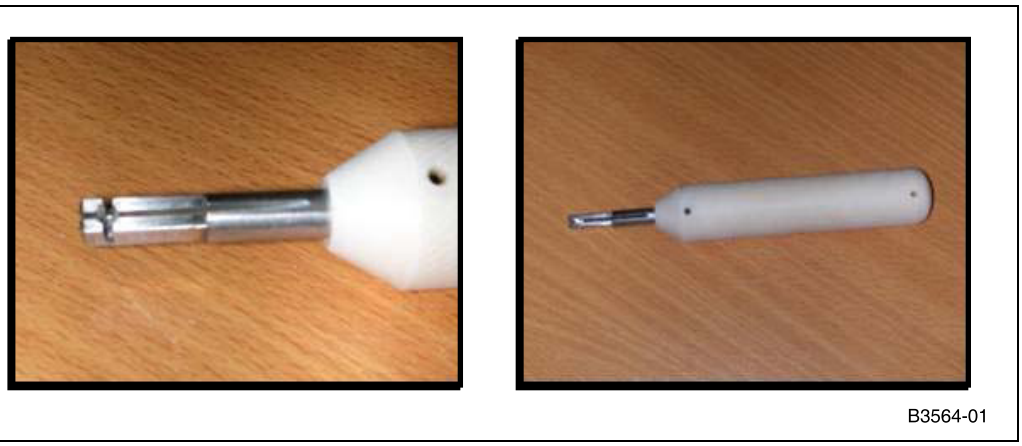


Figure 12. Hand-Tool on Heat-Sink Clip Assembly

6.6 Reliability Guidelines

Each motherboard, heat sink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. Some general recommendations are shown in Table 3.

Table 3. Reliability Guidelines

Test	Requirements	Reference	Pass/Fail Criteria
Mechanical Shock	25G 6 axis shock 2 shock/axis	Unpackaged System Level	Visual Check, Electrical Continuity Test (with cross section information), Thermal Resistance Testing
Random Vibration	2.20 gRMS, 5 Hz @ 0.001 g^2/Hz to 20 Hz @ 0.01 g^2/Hz (slop up) 20 to 500 Hz @ 0.01 g^2/Hz (flat) 10 min/axis	Unpackaged System Level	Visual Check, Electrical Continuity Test (with cross section information), Thermal Resistance Testing
High Operating Temperature	125 °C for 1000 hours	Board-Level Legacy	Visual Check and Electrical Continuity Test
Temperature Cyclic	-40 °C to +85 °C for 1300 cycles	Board-Level Use Condition	Visual Check and Electrical Continuity Test
Humidity	85 °C with 85% RH for 1000 hours	Board-Level Legacy	Visual Check

Appendix A Thermal Solution Component Suppliers

A.1 Reference Thermal Solution Component Suppliers

Table 4. Reference Thermal Solution Component Suppliers

Part	Part Number	Supplier	Contact Information
Unidirectional Fin Heat Sink	C40682-002	Fujikura	Ash Ooe (408) 988-7405 a_ooe@fujikura.com Fujikura America 3001 Oakmead Village Drive Santa Clara, CA 95051-081
Thermal Interface Material	PCM45HD	Honeywell	Honeywell Electronic Materials 17, Changi Business Park Central 1, Singapore 486073 Tel: 65-6580-3530
Heat Sink Clip	C40429-001	Fujikura	Ash Ooe (408) 988-7405 a_ooe@fujikura.com Fujikura America 3001 Oakmead Village Drive Santa Clara, CA 95051-081
Hand Tool Supplier	MID# K-00103	Zoomax	Jason Bong / BG Lee (Marketing Manager & General Manager) Zoomax Engineering 572, Jalan Waja 7, Kawasan Industri Waja II, 09000 Kulim, Kedah H/P#: 012-4282327 Office Tel: 604-4892219 Office Fax: 604-4892290 Email: zoomax@tm.net.my or zoomax@pd.jaring.my

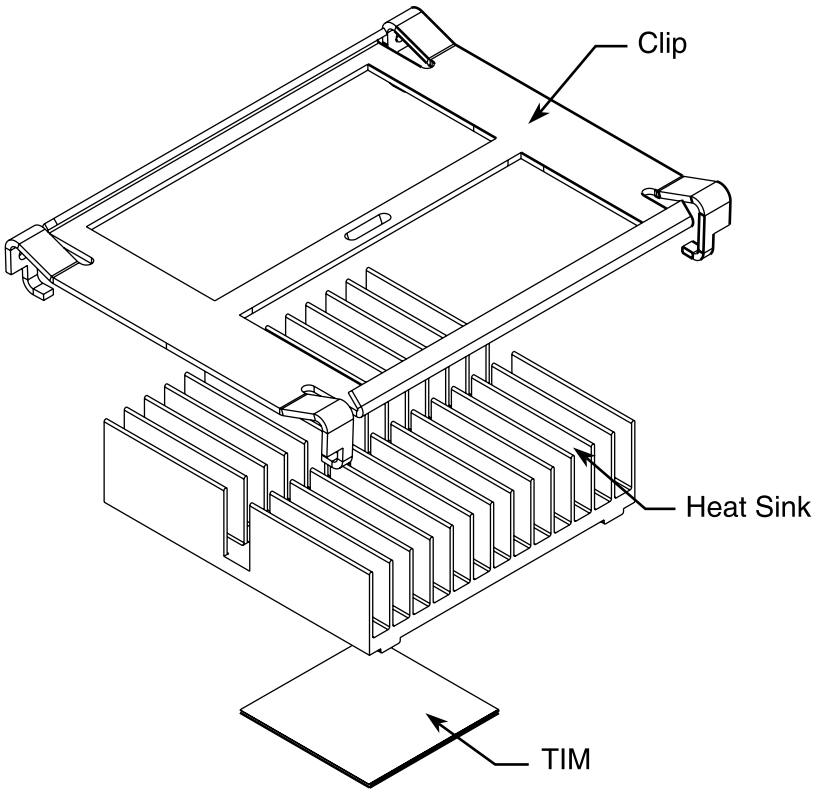
Appendix B Mechanical Drawings

Table 5 lists the mechanical drawings included in this appendix.

Table 5. Mechanical Drawing List

Drawing Description	Figure Number/Location
Intel® 80333 I/O Processor Reference Thermal Solution Assembly Drawing	Figure 13
Heat Sink (C40682-002) and Clip (C40429-001) Schematic Drawings	"Heat Sink Schematic 1" on page 26 "Heat Sink Schematic 2" on page 27 "Clip Schematic 1" on page 29 "Clip Schematic 2" on page 30 "Clip Schematic 3" on page 31

Figure 13. Intel® 80333 I/O Processor Reference Thermal Solution Assembly Drawing



Note: The rails on the heat sink prevent the heat sink from tipping.

The heat sink schematics appear on the following pages:

DWG. NO	SHT.	REV
C40682	1	2

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPROVED
	0	PRELIMINARY RELEASE	12/18/02	VP/CK
	1	RELEASE		
	2	2 SIDE RAILS ADDED	7/21/04	TY HIN

NOTES:

1. INTEL PROCUREMENT SPEC. A02160 SHALL APPLY.
2. REMOVE ALL BURRS. BREAK SHARP EDGES 0.13 MAX.
3. TOOLING REQUIRED TO MAKE THIS PART SHALL BE THE PROPERTY OF INTEL, AND SHALL BE PERMANENTLY MARKED WITH INTEL'S NAME AND APPROPRIATE PART NUMBER.
4. TOOL DESIGN SHALL BE SUBMITTED TO AND APPROVED BY INTEL ENGINEERING PRIOR TO CONSTRUCTION OF THE TOOLS.

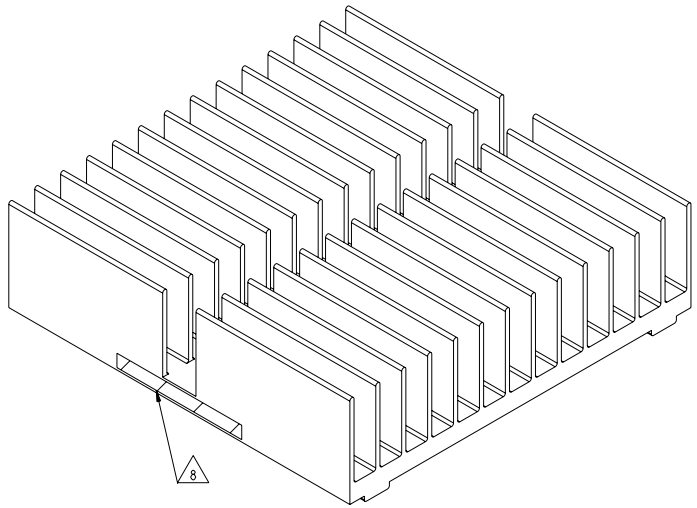
△5 MATERIAL: AL 6063-T5

△6 FINISH: DE-GREASE ONLY.

7. ALL SURFACES ASSOCIATED WITH DATUM "A" SHALL BE FREE OF BURRS.

△8 PART NUMBER SHALL BE CLEARLY MARKED IN REGION SHOWN PER INTEL PART MARKING SPECIFICATION I64997, MARKING METHOD 3.5.

9. (C) INDICATES "CRITICAL TO FUNCTION" DIMENSION.



-003	-002	-001	ITEM NO	PART NUMBER	DESCRIPTION
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
.X ± 0.2 Angles ± 2.5°
.XX ± 0.13

THIRD ANGLE PROJECTION

DESIGNED BY	V. PANDEY	DATE 12/18/02
DRAWN BY	CK. YOON	DATE 12/18/02
CHECKED BY		DATE
APPROVED BY		DATE
MATERIAL:	△5	
FINISH:	△6	

DEPARTMENT ATD

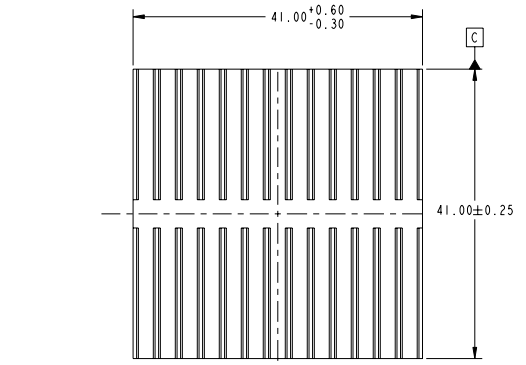
intel © CORP. 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119

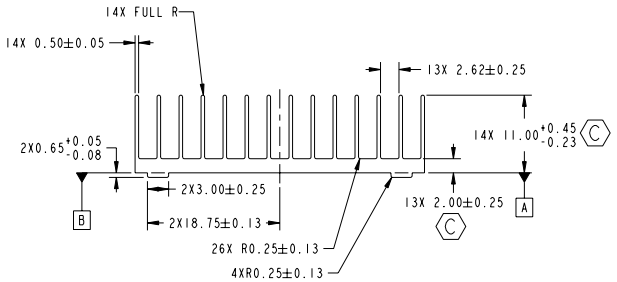
TITLE

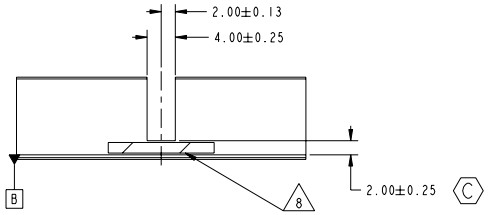
HEATSINK

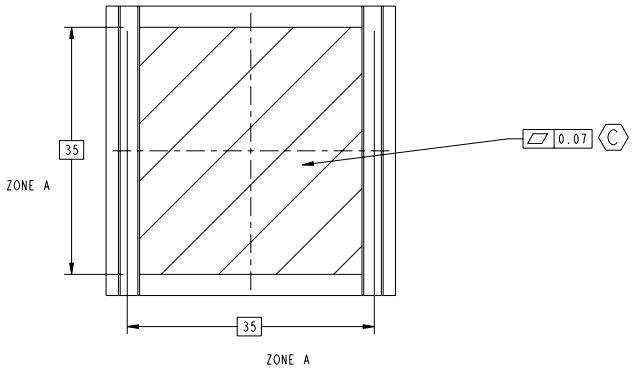
SIZE	CAGE CODE	DRAWING NUMBER	REV
D	34649	C40682	2

SCALE: NONE | DO NOT SCALE DRAWING | SHEET 1 OF 2









DEPARTMENT					
ALUM. 6063-T5	intel® CORP. 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	SIZE D	CAGE CODE X	DRAWING NUMBER C40682	REV 2
		SCALE: 3:1	DO NOT SCALE DRAWING	SHEET 2 OF 2	

The clip schematics appear on the following pages:

- "Clip Schematic 1" on page 29
- "Clip Schematic 2" on page 30
- "Clip Schematic 3" on page 31

DWG. NO	SHT.	REV
C40429	1	1

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPROVED
	1	PRELIMINARY RELEASE	06/10/02	VP

NOTES:

1. INTEL PROCUREMENT SPEC. A02160 SHALL APPLY.
2. REMOVE ALL BURRS. BREAK SHARP EDGES 0.13 MAX.
3. TOOLING REQUIRED TO MAKE THIS PART SHALL BE THE PROPERTY OF INTEL, AND SHALL BE PERMANENTLY MARKED WITH INTEL'S NAME AND APPROPRIATE PART NUMBER.
4. TOOL DESIGN SHALL BE SUBMITTED TO AND APPROVED BY INTEL ENGINEERING PRIOR TO CONSTRUCTION OF THE TOOLS.
5. MATERIAL
   0.8±0.025 STAINLESS STEEL, HALF HARD
   AMS 5518 ASTM A666)
6. DE-GREASE AND REMOVE OIL/DIRT MARKS.
7. (C) INDICATES "CRITICAL TO FUNCTION" DIMENSION.
8. PART NUMBER SHALL BE CLEARLY MARKED IN REGION SHOWN PER INTEL PART MARKING SPECIFICATION 164997, MARKING METHOD 3.5.
9. ALL DIMENSIONS TO THEORETICAL INTERSECTIONS.

-003	-002	-001	ITEM NO	PART NUMBER	DESCRIPTION
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND TOLERANCES
IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
.X ± 0.2 Angles ± 5.0°
.XX ± 0.13

THIRD ANGLE PROJECTION

DESIGNED BY	V.PANDEY	DATE 06/10/02
DRAWN BY	CK,YOON	DATE 06/10/02
CHECKED BY		DATE
APPROVED BY		DATE
MATERIAL:	5	
FINISH:	6	

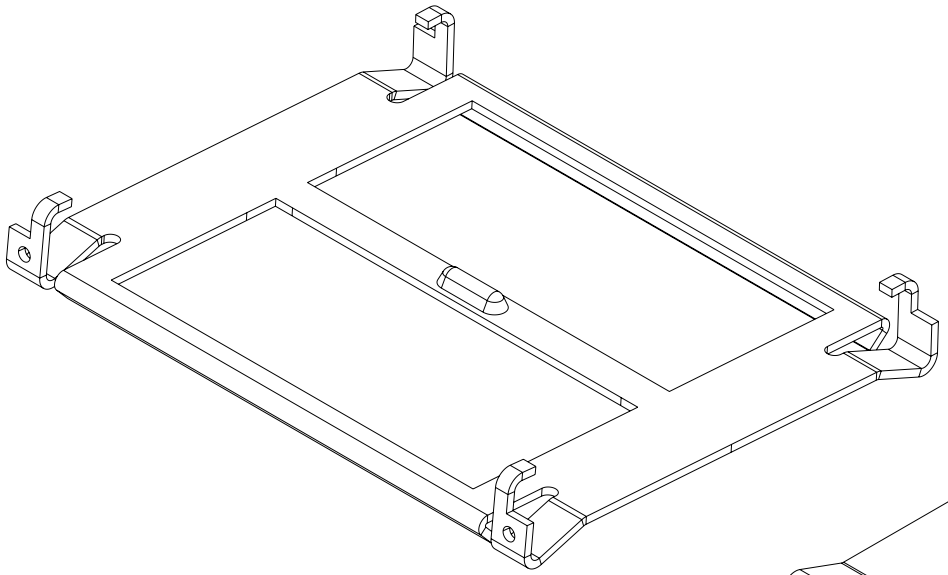
DEPARTMENT
***
intel CORP. 2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

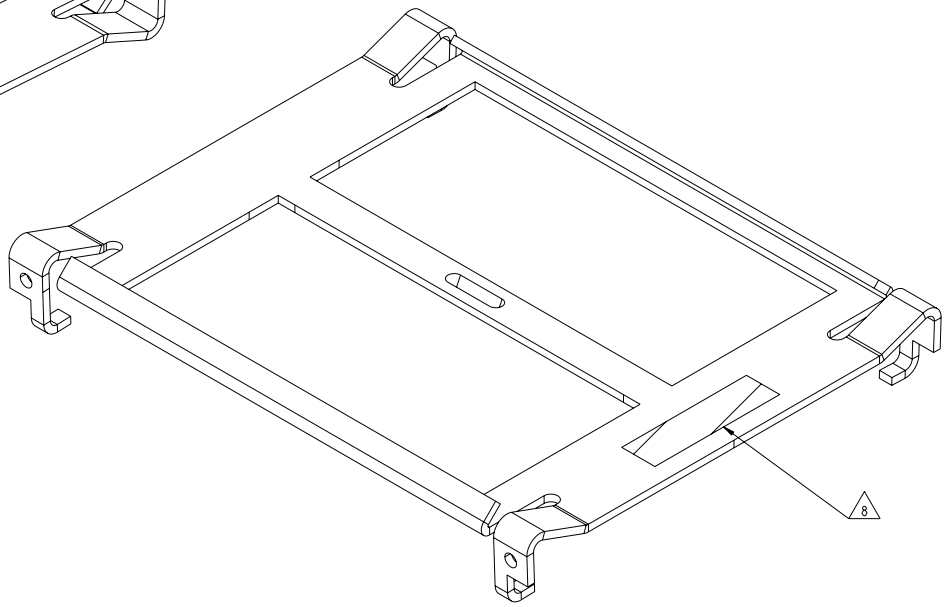
TITLE

CLIP

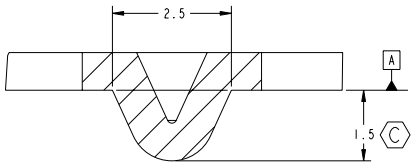
SIZE	CAGE CODE	DRAWING NUMBER	REV
D	34649	C40429	1

SCALE: NONE | DO NOT SCALE DRAWING | SHEET 1 OF 3





DEPARTMENT ...	intel® CORP. 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	SIZE D	CAGE CODE 34649	DRAWING NUMBER C40429	REV 1
		SCALE: NONE	DO NOT SCALE DRAWING	SHEET 2 OF 3	



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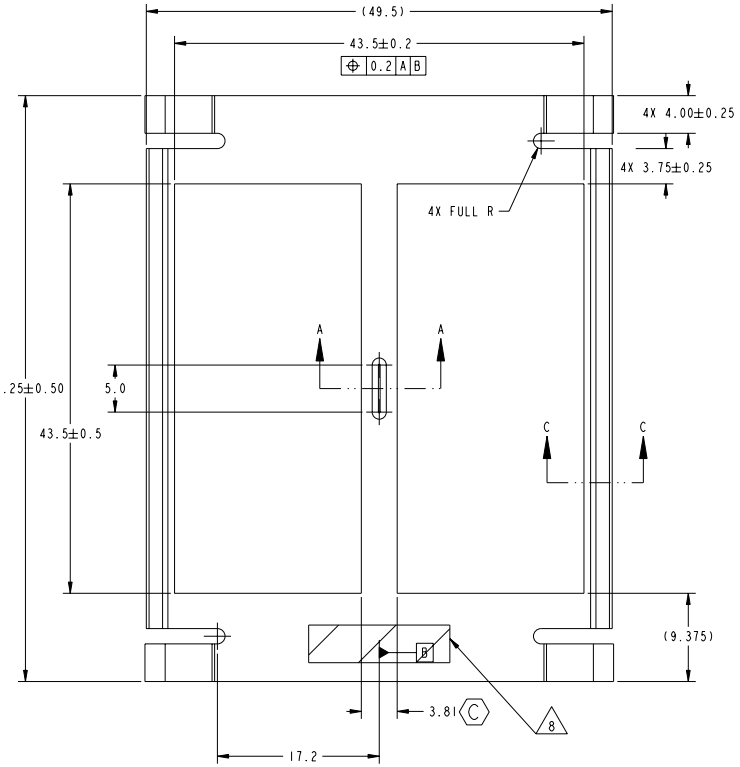

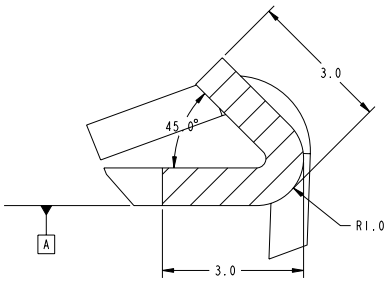

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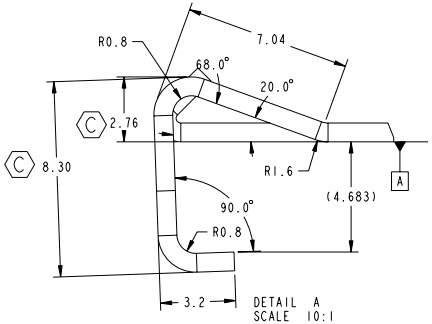
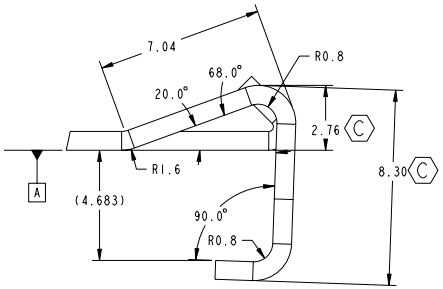
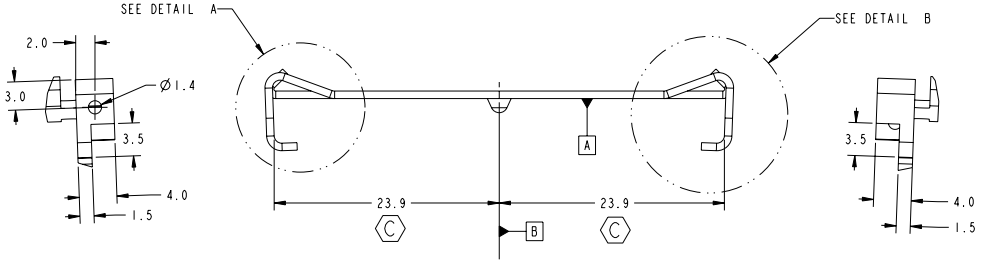


DETAIL A
SCALE 10:1



DETAIL B
SCALE 10:1



DEPARTMENT					
ATD	intel® CORP. 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	SIZE D	CAGE CODE 34649	DRAWING NUMBER C40429	REV I
		SCALE: 4:1	DO NOT SCALE DRAWING	SHEET 3 OF 3	

Appendix C Design Validation (DV)

C.1 TIM Degradation Shock and Vibration Validation Strategy

C.1.1 TIM Degradation

TIM degradation is checked through thermal resistance (Rjs) between die and heat sink at a given package power and ambient settings. Definition is given by Equation 2.

Equation 2. Thermal Resistance

$$\text{Thermal Resistance, } R_{js} = \frac{T_{Junction} - T_{Sink}}{Power} \bullet A_{die}$$

C.1.2 Metrology

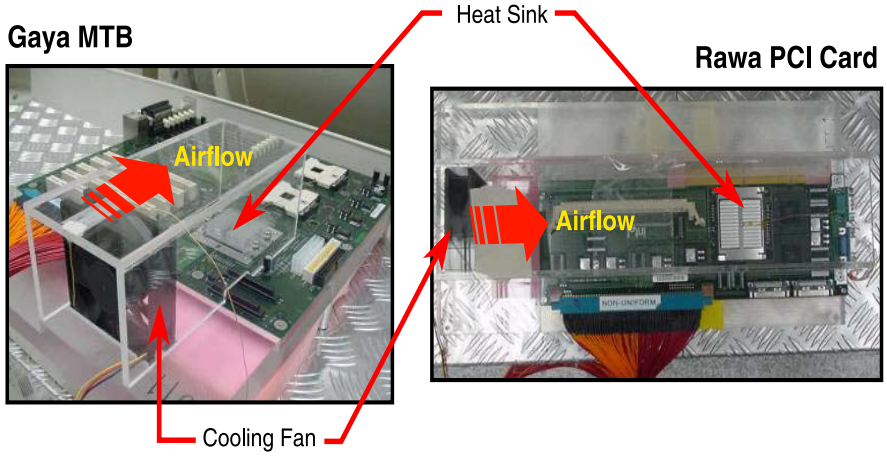
- Thermocouple is attached at the top of the heat sink base, between the center fins, to measure the heat sink temperature, T_S.
- Units are measured twice: before and after stress. Test parameters are identical for both of these tests.

C.1.3 TIM Thermal Resistance

- Die temperature is higher and heat sink temperature is lower.
- Primary cause is increase in TIM bond line thickness, due to delamination.

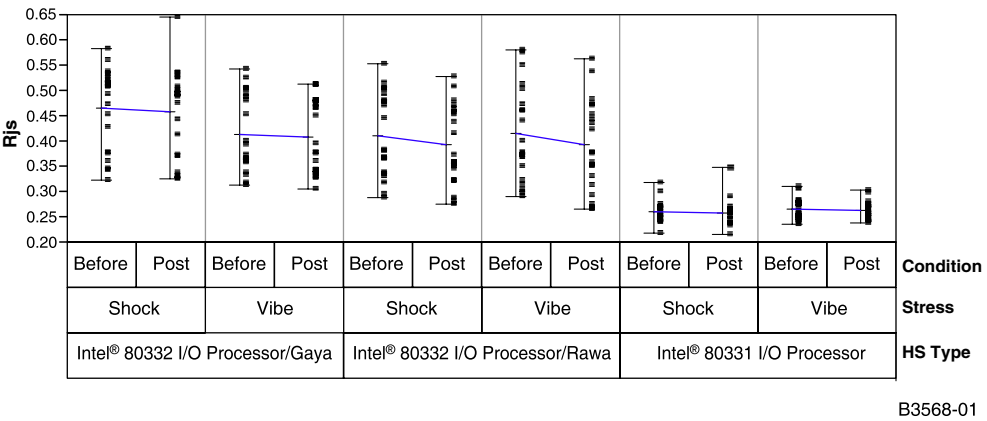
C.1.4 Test Set-up

Figure 19. Test Fixture



C.1.5 DV Result Summary

Figure 20. Variability Chart for Rjs



Appendix D Manufacturing Validation (MV)

Table 6. Intel® 80333 I/O Processor Clip MV Result Summary

MV Indicators	Description	Success Criteria	Result Summary	Pass/Fail
Static Preload Force	Preload Force vs. Specification	6–25 lbs.	15.46 ± 3.37 lbs.	Pass
Transient Load	Maximum preload force recorded during enabling assembly	< 40 lbs.	< 33 lbs.	Pass
Assembly Yield	Post 1× Enabling Assembly and Disassembly	All pass IWS criteria (98.5% @ 60% CL)	100%	Pass
Rework Yield	Post 3× Rework Enabling Assembly and Disassembly	All pass IWS criteria (90% @ 60% CL)	100%	Pass
E-test	Time 0	100% Electrical Pass (98.5% @ 60% CL)	100%	Pass
	Post 3× Rework Enabling Assembly and Disassembly	100% Electrical Pass (90% @ 60% CL)	100%	Pass
X-section	Time 0	No solder crack	No Solder Crack	Pass
	Post 3× Rework Enabling Assembly and Disassembly	No solder crack	No Solder Crack	Pass
Die Crack DOE	Check for die crack caused by enabling	No die crack	No Die Crack	Pass
Local Cell MCA	Load Cell Capability Study	P/T <= 30%	P/T = 1.6% << 30%	Pass
Beat Rate	Baseline	NA	65 UPH	NA

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