Intel® 80321 I/O Processor Software Conversion to Intel® 80331 I/O Processor

Application Note

September 2003

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Revision History

Date	Revision	Description
September 2003	001	Initial Release.

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1.0 Objective

This document defines the software differences between the Intel® 80321 I/O processor (80321) and Intel® 80331 I/O processor (80331). It also includes the software differences for the PCI-X bridge integrated in the 80331.

Note: As with any design change, customers need to perform thorough validation of their application hardware and software prior to production.

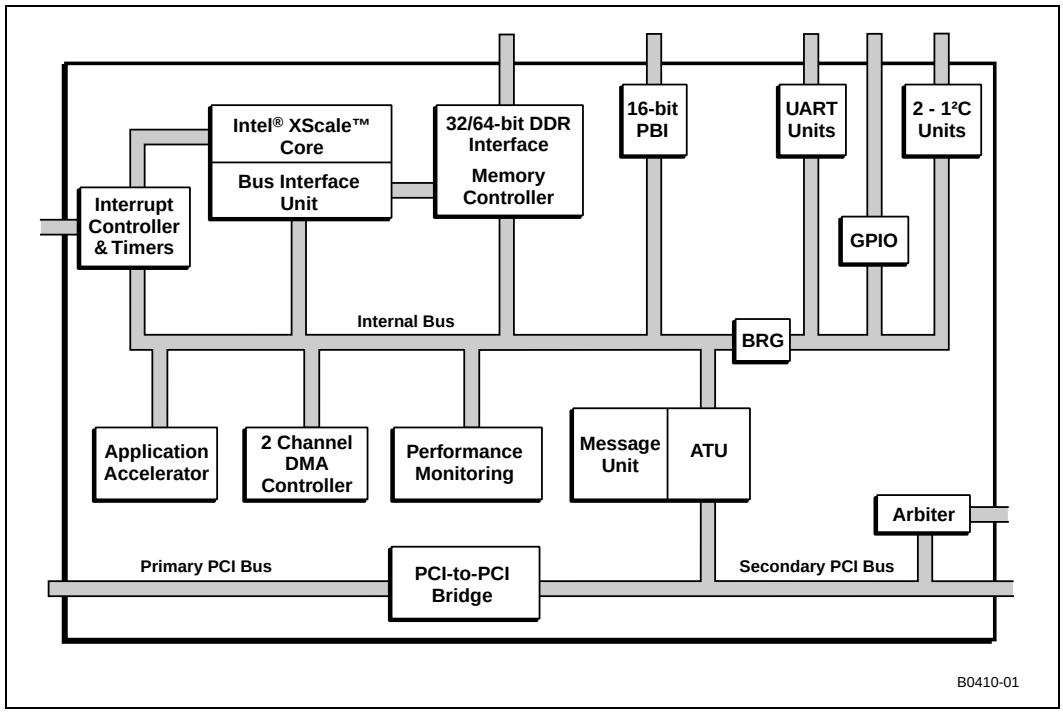
2.0 Intel® 80331 I/O Processor

The 80331 is the first Intel I/O processor with an integrated Intel® Xscale™ core, memory controller and PCI-X to PCI-X bridge. The key improvements over the 80321 provided in the 80331 include:

- higher speed core
- dual-ported memory controller architecture
- higher speed memory
- higher speed internal bus
- higher performance interrupt controller

Core speeds are available in 500 MHz, 667 MHz and 800 MHz. The memory controller is dual-ported and supports DDR333 and DDR-II 400.

Figure 1. Intel® 80331 I/O Processor Block Diagram



3.0 Intel® 80331 I/O Processor Memory Controller Architecture

The 80331 made significant improvements to the memory controller of the 80321, in both architecture and speed. The 80331 memory controller supports both DDR333 SDRAM for 2.7 GB/s bandwidth and DDR-II 400 MHz SDRAM for 3.2 GB/s bandwidth. The memory technology and speed are selectable via a reset strap (MEM_TYPE).

Note: DDR333 can only be used with the 80331 500 MHz and 667 MHz. DDR-II 400 can only be used with the 80331 500 MHz and 800 MHz. Only the 80331 500 MHz supports both memory technologies.

The architecture of the 80331 implements a dual-ported memory controller and Intel® Xscale™ core bus interface unit. This architecture allows core transactions targeting SDRAM to pass directly to the MCU, without crossing the Internal Bus. The memory controller also supports pipelined SDRAM transactions, to reduce latency of back-to-back transactions. The MCU implements a programmable arbiter, allowing users to optimize the MCU behavior to best serve their application needs.

Core processor transactions, targeting peripheral units or PCI devices, are directed across the Internal Bus by the Intel® Xscale™ core Bus Interface Unit. Peripheral units also have a separate port to the MCU for transactions, which are prioritized in the MCU against core processor transactions.

3.1 MCU Software Changes to Intel® 80321 I/O Processor

The new 80331 MCU has additional registers for control of the arbiter and additional features. Control for both DDR and DDR-II impacts some register contents. Many registers remain unchanged, however the internal bus addresses of the registers have been moved to accommodate additional registers.

Note: The 80331 MCU is not backward compatible to the 80321.

Existing 80321 SDRAM initialization software needs modification to align register addresses to the 80331 MCU MMR map and modify the method for initializing SDRAM through Initialization and Control Registers. The DDR SDRAM drive strength and I/O control registers are revised from the 80321. Two new MCU interrupt sources in the MCISR require interrupt service routines for the MCU to be updated. Registers that have control bits added or changed include (see Table 1):

Table 1. MCU Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
SDIR	SDRAM Initialization	Modified bit definition. Default: n/a
SDCR[1:0]	SDRAM Control	Added new fields and split into two registers. Default: n/a
S32SR	SDRAM 32-bit Region Size	New Register for new feature. Default: disabled
MCISR	Interrupt Status Register	New bits. Default: no error
MPTCR	MCU Port Transaction Count Register	New register for dual-ported MCU. Default: IB=1, Core=12
MPCR	MCU Preemption Control	New register for dual-ported MCU. Default: disabled.
various	I/O Drive Strength and Delay Control Registers	New MMR addresses and new definition

3.2 BIU Software Changes to Intel® 80321 I/O Processor

The new BIU of the 80331 has changed from the 80321 to implement the dual-port architecture of the new MCU. The registers of the BIU remain unchanged with the exception of addresses. The BIU registers of the 80331 are only accessible as memory mapped registers and not as co-processor registers, as was the case in the 80321. An additional register also exists for control of the BIU in 80331.

Note: The 80331 BIU is not backward compatible to the 80321.

Existing 80321 software needs to be modified to align register addresses to the 80331 BIU MMR map, instead of co-processor addressable registers. In addition, the following registers of the BIU have been changed or added as described in Table 2:

Table 2. BIU Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
BIUSR	BIU Status	New bits added
BIUCR	BIU Control	New register for dual-ported MCU

4.0 Intel® 80331 I/O Processor Interrupt Controller Architecture

The Interrupt Controller Unit (ICU) in the 80331 enhances what was implemented in the 80321. The 80331 ICU includes a vector port for both FIQ and IRQ interrupt, allowing the interrupt service routine to directly read the interrupt service routine vector, saving software overhead. The vector is calculated by the ICU, based on programmed values for Interrupt Service Routine Base Address, Interrupt Service Routine Size, and interrupt priorities. The 80331 ICU supports 64 interrupt sources (not all 64 sources are used) as compared to 32 in 80321.

4.1 ICU Software Changes to Intel® 80321 I/O Processor

The advanced vector generation features of the 80331 ICU are accessible by additional registers. An additional thirty-two interrupt sources are supported in 80331 and a second set of registers for Control, Status and Steering exists in 80331 with the sources divided across these registers. The 80331 ICU registers exist as both MMR mapped and Co-processor 6 registers as in the 80321, however, the ICU registers are remapped to different addresses.

Note: The 80331 BIU is not backward compatible to the 80321.

Existing 80321 software can be modified to take advantage of the interrupt vector generation feature utilizing the following registers of the ICU which have been added:

Table 3. ICU Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
INTCTL[1:0]	Interrupt Mask	Two registers for additional sources
INTSTR[1:0]	Interrupt Steering	Two registers for additional sources
IINTSRC[1:0]	IRQ Pending Interrupt Sources	Two registers for additional sources
FINTSRC[1:0]	FIQ Pending Interrupt Sources	Two registers for additional sources
IPR[3:0]	Interrupt Priority	New Registers for interrupt priorities
INTBASE	Interrupt Service Routine Base Address	New Registers for vector generation
INTSIZE	Interrupt Service Routine Size	New Registers for vector generation
IINTVEC	IRQ Interrupt Vector	New Registers for vector generation
FINTVEC	FIQ Interrupt Vector	New Registers for vector generation
PIRSR	PCI Interrupt Routing Select Register	New bits for additional interrupt steering flexibility

5.0 Private Device Control Architecture

Private devices are hidden from host PCI configuration software, but are configurable through the ATU. To configure the 80331 for private device control, the PCI-to-PCI bridge must be configured to enable private Type 0 commands and private memory space on the secondary PCI bus. These capabilities are enabled by hardware via two reset straps: PRIVDEV and PRIVMEM.

Private devices can be initially configured in the 80331 through the PRIVDEV reset strap. Pulling this input pin high, on the rising edge of reset, causes the Secondary IDSEL Select Register (SISR) bits to default to one, resulting in device numbers 0 through 9 (devices with IDSEL tied to S_AD[25:16]) to be hidden from the Primary PCI interface.

Note: Software can check this configuration by reading PCSR.3.

Private memory can be initially configured in the 80331 through the PRIVMEM reset strap. Pulling this input pin high, on the rising edge of reset, causes the Secondary Decode Enable Register bit 2 (SDER.2) to default to one creating a private memory space on the secondary PCI bus that allows peer-to-peer transactions. Software can check this configuration by reading PCSR.0 or SDER.2.

The 80331 uses the same registers as the 80321 to initiate configuration cycles:

- Outbound Configuration Cycle Address Register (OCCAR)
- Outbound Configuration Cycle Data Register (OCCDR).

Note: The 80331 private device control mechanism is not backward compatible to RAIDIOS used with the 80321.

Existing 80321 software needs to be modified to utilize the 80331 private device control mechanism. The following registers have been added as described in Table 4:

Table 4. Private Device Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
PCSR.0	Private Memory Enable	New bit function controlled by PRIVMEM.
PCSR.3	Private Device Enable	New bit function controlled by PRIVDEV.
SDER.2	Secondary Decode Enable Register	New registers reside in the bridge and are not accessible from the ATU.
SISR	Secondary IDSEL Select Register	

6.0 Peripheral Bus Interface

The Peripheral Bus Interface (PBI) of the 80331 is 16-bits wide, and includes two address windows.

Note: The PBI programming interface is backward compatible to the 80321 for the registers and features except windows 2-5.

The programming difference between the 80321 and the 80331 for the PBI interface is limited to the following registers, as shown in Table 5.

Table 5. PBI Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
PBBAR[2-5]	Peripheral Bus Base Address Registers	Not implemented in the 80331
PBLR[2:5]	Peripheral Bus Limit Registers	Not implemented in the 80331
PBDSCR	PBI I/O Drive Strength	New MMR address

7.0 Address Translation Unit

The 80331 ATU has several differences compared to the 80321 ATU. These include:

- Additional capability (VPD – Vital Product Data)
- Removal of the PCI bus pad control
- Modification to the PIRSR

A PCI Vital Product Data extended capability has been added to the Address Translation Unit of the 80331. The registers for this capability are added to the ATU MMR map. The PCI Interrupt Routing Select register has been remapped in 80331 with additional bits to handle more interrupts and steering options. The PCI Bus Drive Strength Control register is removed from the ATU and the bus pad control is redefined in a dedicated register group. ATU Configuration Write Interrupt is a new interrupt source and there are three new bits in the ATUIMR and ATUISR to support this interrupt.

Table 6 lists the registers which are changed in the 80331 from the 80321.

Table 6. ATU Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
VPD_Cap_ID	VPD capability ID	New register in ATU for optional capability
VPD_Next_Item_Ptr	VPD Next capability Pointer	New register in ATU for optional capability
VPDAR	VPD Address Register	New register in ATU for optional capability
VPDDR	VPD Data Register	New register in ATU for optional capability
PIRSR	PCI Interrupt Routing Select Register	New MMR address, and additional bits
various	PCI Bus Drive Strength Control Registers	New MMR address and definition
PCSR.0	Private Memory Enable	New bit function controlled by PRIVMEM.
PCSR.3	Private Device Enable	New bit function controlled by PRIVDEV.
PCSR.4	Reset Peripheral Bus control bit	Not implemented in the 80331 ATU
ATUCMD.10	Interrupt Disable bit	New bit to support *PCI Local Bus Specification*, Revision 2.3
ATUSR.3	Interrupt Status bit	New bit to support *PCI Local Bus Specification*, Revision 2.3
ATUISR.15,17	ATU Interrupt Status Register	New Status bits to support ATU Config Reg Write Interrupt.
ATUIMR.12,14	ATU Interrupt Mask Register	New Mask bits to support ATU Config Reg Write Interrupt

8.0 GPIO and Serial Interfaces

The 80331 includes eight GPIOs, two backward compatible I^2C interfaces and two UARTs.

8.1 GPIO

The eight GPIOs are multiplexed with the serial interfaces as in the 80321. The 80331 GPIOs are MUXed with UART signals, but the 80321 GPIOs are MUXed on I^2C. The GPIO registers are remapped out of the Interrupt Control Unit MMR section.

Table 7. GPIO Register Changes from Intel® 80321 I/O Processor

Register	Description	Change
GPOE	GPIO Output Enable Register	New MMR Address
GPID	GPIO Input Data Register	New MMR Address
GPOD	GPIO Output Data Register	New MMR Address

8.2 I^2C Interface

80331 integrates two I^2C interfaces that are backward compatible to the 80321. These are unchanged in function and register address, but use dedicated pins (not shared with GPIOs).

8.3 UART Units

These units are mapped to MMR space, and are 4-pin UARTs (RXD, TXD, CTS# and RTS#) which are multiplexed with four GPIOs each. The registers for the the 80331 UARTs are listed in Table 8.

Note: Two UARTs are integrated in the 80331 that did not exist in the 80321.

Table 8. UART Registers

Register	Description	Change
UxRBR	UART Receive Buffer	New Register. x = 0 or 1
UxTHR	UART Transmit Buffer	New Register. x = 0 or 1
UxIER	UART Interrupt Enable	New Register. x = 0 or 1
UxIIR/UxFCR	UART Interrupt Status (Rd)/UART FIFO Control (Wr)	New Register. x = 0 or 1
UxLCR	UART Line Control	New Register. x = 0 or 1
UxMCR	UART Modem Control	New Register. x = 0 or 1
UxLSR	UART Line Status	New Register. x = 0 or 1
UxMSR	UART Modem Status	New Register. x = 0 or 1
UxSPR	UART Scratch Pad	New Register. x = 0 or 1
UxDLL	UART Divisor Latch Low	New Register. x = 0 or 1
UxDLH	UART Divisor Latch High	New Register. x = 0 or 1
UxFOR	UART FIFO Occupancy	New Register. x = 0 or 1
UxABR	UART Autobaud Control	New Register. x = 0 or 1
UxACR	UART Autobaud Count	New Register. x = 0 or 1

9.0 Other Integrated Peripherals

The 80331 includes a complete set of peripherals for RAID software matching that of the 80321, which include (These units remain unchanged in the 80331):

- Timers
- DMA
- AAU
- MU

The DMA does support a 32-bit CRC generation engine. This is a new feature over the 80321 and includes some register changes, but does remain backwards compatible. CRC32-C is an algorithm required for iSCSI applications.

10.0 Intel® 80331 I/O Processor PCI-X to PCI-X Bridge

The 80321 does not have an integrated PCI-X to PCI-X bridge, therefore, in order to use the 80321 in an add-in card application, a PCI-X to PCI-X bridge is required. A PCI-X Bridge is commonly used by customers and in this section is compared to the integrated PCI-X to PCI-X bridge in 80331.

The bridge programming interface is provided only in the configuration register address space, which is accessible from the primary PCI bus interface.

Note: The bridge registers are not accessible by the Intel® Xscale™ core.

10.1 Standard Configuration Header (0-3Fh)

According to the *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1, a bridge must implement a 256-byte configuration space. The first 64 bytes must adhere to a predefined header format. The remaining 192 bytes may be used for device specific purposes. For both bridges the configuration registers are accessible only from the primary PCI bus, using configuration reads and writes.

Table 9. Comparison of First 64 Bytes (0-3Fh) of Configuration Header (Sheet 1 of 2)

Address Offset	Register	PCI-X Bridge Reset Value	Intel® 80331 I/O Processor Reset Value	Difference Description
00h	Vendor ID	1014h	8086h	1
02h	Device ID	01A7h	0335h	1
04h	Command	0000h	0000h	
06h	Status	02B0h (PCI) 0230h (PCI-X)	02B0h	2
08h	Revision ID	02h	00h	1
09h	Class code	060400h	060400h	
0Ch	Cache Line Size	00h	00h	3
0Dh	Latency Timer	00h (PCI) 40h (PCI-X)	00h (PCI) 40h (PCI-X)	
0Eh	Header Type	01h	01h	
0Fh	BIST	00h	Reserved	
10h	BAR0	00h (BAR_EN=0) 0Ch (BAR_EN=1)	Reserved	4
14h	BAR1	00h	Reserved	4
18h	Primary Bus #	00h	00h	
19h	Secondary Bus #	00h	00h	
1Ah	Subordinate Bus #	00h	00h	
1Bh	Secondary Latency Timer	00h (PCI) 40h (PCI-X)	00h (PCI) 40h (PCI-X)	
1Ch	IO Base	x1h	01h	
1Dh	IO Limit	x1h	01h	
1Eh	Secondary Status	02A0h (PCI) 0220h (PCI-X)	02A0h	5
20h	Memory Base	8000h	0000h	6

Table 9. Comparison of First 64 Bytes (0-3Fh) of Configuration Header (Sheet 2 of 2)

Address Offset	Register	PCI-X Bridge Reset Value	Intel® 80331 I/O Processor Reset Value	Difference Description
22h	Memory Limit	0000h	0000h	
24h	Prefetchable Memory Base	8001h	0101h	7
26h	Prefetchable Memory Limit	0001h	0001h	
28h	Prefetchable Base Upper 32	00h	00h	
2Ch	Prefetchable Limit Upper 32	00h	00h	
30h	I/O Base Upper 16	00h	00h	
32h	I/O Limit Upper 16	00h	00h	
34h	Capabilities Pointer	80h	D4h	8
38h	Expansion ROM Base Address	Reserved	Reserved	
3Ch	Interrupt Line	xxh	00h	9
3Dh	Interrupt Pin	00h	00h	
3Eh	Bridge Control	00h	00h	

NOTES:

1. The vendor, device and revision IDs are all different to ensure uniqueness between manufacturers and products.
2. Bit 7 = Fast Back to Back Capable. Section 7.1 of *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a states “This bit is allowed to have any value when the device is in PCI-X mode. (PCI-X devices never use fast back-to-back timing, regardless of the state of this bit.)
3. The PCI-X bridge supports cache lines of 4, 8, 16 and 32. 80331 supports cache lines of 8 and 16. Page 181 in the *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a states “The contents of this register are ignored by an interface in PCI-X mode.”
4. 80331 does not implement BARs. Section 3.2.5.1 in the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1 states “The base address registers are optional registers used to map internal (device-specific) registers into memory or I/O spaces.”
5. Bit 7 = Fast Back to Back Capable. Page 182 of the *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a states “This bit must be set to 0 in PCI-X mode”.
6. Section 3.2.5.8 in the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1 states “These registers must be initialized by configuration software so default states are not specified.”
7. Section 3.2.5.9 in the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1 states “These registers must be initialized by configuration software so default states are not specified.”
8. Capability Lists are not located at the same offsets. See Extended Capability Lists section.
9. Section 3.2.5.15 in the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1 states “This register must be initialized by initialization code so a default state is not specified” and “If a bridge does not implement an interrupt signal pin, the POST (power-on self test) code must write FFh to this register.”

10.2 Extended Capability Lists

The 80331 supports two extended capabilities:

- PCI-X
- Power Management

The PCI-X bridge supports two extended capabilities:

- PCI-X
- Power Management

These extended capability lists are not located at the same offsets.

Table 10. Comparison of PCI-X Extended Capability List

Register	PCI-X Bridge		Intel® 80331 I/O Processor		Difference Description
	Address Offset	Reset Value	Address Offset	Reset Value	
PCI-X ID	80h	07h	F0h	07h	
Next Capability Pointer	81h	90h	F1h	00h	1
PCI-X Secondary Status	82h	0003h	F2h	0xx3h	2
PCI-X Bridge Status	84h	0003 00F8h	F4h	000x 00F8h	
Upstream Split Transaction	88h	0020 0020h	F8h	003E 003Eh	3
Downstream Split Transaction	8Ch	0020 0020h	FCh	003E 003Eh	3

NOTES:
1. This is the first capability list for the PCI-X bridge and the last for the 80331.
2. Bits 8:6 depend on the operating frequency of the secondary PCI bus.
3. The capacity field for the PCI-X bridge indicates that there are 32 ADQs (4K bytes) available for buffer space. For the 80331, the bridge essentially has infinite capacity. The Limit field for the PCI-X bridge is the same as the capacity field. For the 80331, the limit is not used by the bridge.

Table 11. Comparison of Power Management Extended Capability List

Register	PCI-X Bridge		Intel® 80331 I/O Processor		Difference Description
	Address Offset	Reset Value	Address Offset	Reset Value	
Power management ID	90h	01h	DCh	01h	
Next Capability Pointer	91h	00h	DDh	F0h	1
Power management capabilities	92h	0002h	DEh	0202h	2
Power management control/status	94h	0000h	E0h	0000h	
Bridge support extensions	96h	00h	E2h	00h	
Data Register	97h	00h	E3h	00h	

NOTES:
1. This is the last capability list for the PCI-X bridge and the second for the 80331.
2. The PCI-X bridge does not support the D1 power state, and the 80331 does support D1 power state.

10.3 Device Specific Registers

The 80331 has 14 device specific registers. These registers reside in the bridge PCI configuration address space with an offset range of 40h – CBh.

The PCI-X bridge has 18 device specific registers. These registers reside in the bridge PCI configuration address space with an offset range of 40h – 7Fh and B0h-B9h.

Since these registers are device specific, there is very little commonality between the two bridges. There are 17 addresses that overlap between the two bridges. Each of these registers must be analyzed individually by the software programmer.

Gray blocks in Table 12 are 'Reserved' fields.

Table 12. Comparison of Device Specific Registers (Sheet 1 of 2)

Address Offset	PCI-X Bridge	Reset Value	Intel® 80331 I/O Processor	Reset Value
40h	Primary Data Buffering Control	0020h		
41h			Secondary Arbiter Control/Status	F000h
42h	Secondary Data Buffering Control	0020h		
43h			Bridge Control 0	00h (RETRY = 0) 02h (RETRY = 1)
44h	Miscellaneous Control	03h (P_CFG_BUSY = 0) 07h (P_CFG_BUSY = 1)	Bridge Control 1	0020h
45h				
46h			Bridge Control 2	003Fh 001Fh 0007h *Depends on secondary bus clock.
47h				
48h			Bridge Status	0000h
49h				
4Ah-4FH	Reserved			
50h	Arbiter Mode	0800h (S_INT_ARB_EN# = 0) 0801h (S_INT_ARB_EN# = 1)	Multi-Transaction Timer	00FFh
51h				
52h			Read Prefetch Policy	010Fh
53h				
54h	Arbiter Enable	7Fh	P_SERR# Assertion Control	0000h
55h				
56h			Pre-boot Status	0xh
57h	Reserved			
58h	Arbiter Priority	01h	Secondary Decode Enable	FFFAh
59h				
5Ah	Reserved			
5Bh				

Table 12. Comparison of Device Specific Registers (Sheet 2 of 2)

Address Offset	PCI-X Bridge	Reset Value	Intel® 80331 I/O Processor	Reset Value
5Ch	SERR# Disable	00h	Secondary IDSEL Select	xxxxh *Depends on PRIVDEV
5Dh				
5Eh	Reserved			
5Fh				
60h	Primary Retry Counter	0000 0000h	Primary Bridge Interrupt Status	0000 0000h
61h				
62h				
63h				
64h	Secondary Retry Counter	0000 0000h	Secondary Bridge Interrupt Status	0000 0000h
65h				
66h				
67h				
68h	Discard Timer Control	00h		
69h-6Bh	Reserved			
6Ch	Retry and Timer Status	00h		
6Dh-6Fh	Reserved			
70h	Opaque Memory Enable	00h (OPAQUE_EN = 0) 01h (OPAQUE_EN = 1)		
71h-73h	Reserved			
74h	Opaque Memory Base	0001h		
75h				
76h	Opaque Memory Limit	FFF1h		
77h				
78h	Opaque Memory Base Upper 32	FFFF FFFFh		
79h				
7Ah				
7Bh				
7Ch	Opaque Memory Limit Upper 32	FFFF FFFFh		
7Dh				
7Eh				
7Fh				
B0h	Secondary Bus Private Device Mask	0000 0000h (IDSEL_REROUTE_EN = 0) 22F2 0000h (IDSEL_REROUTE_EN = 1)		
B1h				
B2h				
B3h				
B4h-B7h	Reserved			
B8h	Miscellaneous Control 2	0000h		
B9h				

11.0 Summary

The 80331 integrates a PCI-X to PCI-X bridge with an I/O processor. Some programming differences do exist between the 80331 and the 80321, with an PCI-X bridge, as detailed in this document. These include programming interface changes to the:

- BIU
- MCU
- ICU
- ATU
- PBI
- PCI-X to PCI-X bridge

The DMA also includes a new 32-bit CRC generation engine to support iSCSI applications.

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